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Modernization and Removal of Obsolescence in Introductory Digital Electronics Laboratory

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Abstract – Experiments in digital electronics are mandatory part of undergraduate engineering education in many electronics, instrumentation, computer science, information technology, electrical and related branches. Many of these branches have an introductory circuit level course followed by a systems level course.Traditionally, in the introductory circuit level course laboratory, the experiments are performed using the 74 series of TTL ICs that have been available for more than forty years. However, these ICs reached 'end of life' quite some time ago and in near future, their lack of availability will be a common problem. This poses serious questions on the viability of conducting digital electronics laboratory experiments, unless alternative solutions are found. We have designed and built an inexpensive experiment platform based on a Complex Programmable Logic Device (CPLD) from Xilinx that can be used with a wide variety of on-board peripherals. To achieve a low cost solution, a USB to JTAG bridge, necessary to program the CPLD, has been implemented using a RISC microcontroller. This experiment platform called 'AkshayaPatra' can also be used with schematic entry method, which makes it appropriate for an introductory circuit level laboratory.

Keywords – 74-series TTL, CPLD, Digital Electronics, Engineering Education, Programmable Logic Devices

I. INTRODUCTION

Digital Electronics is a mandatory part of undergraduate engineering courses in multiple disciplines – electronics, instrumentation, computer science, information technology, electrical and other allied disciplines [1]-[4]. The laboratory component of a typical introductory level digital electronics course consists of experiments performed using logic gates and other logic blocks such as adders, flip-flops etc. These experiments are typically performed using the 74 series of TTL Logic ICs, which have been commercially available since 1966. However, the 74 series, which once comprised of over 600 different ICs with various logic functions, have reached their "end of life" stage and are no longer in commercial production. This has resulted in increased prices of 74 series devices, due to the scarcity of their supply.The expected lack of availability of 74 series ICs poses a serious challenge in conducting experiments in fundamental digital electronics laboratories. Several approaches suggest the use of computer aided simulations or virtual instrumentation based laboratories as a potential replacement for these experiments [5]-[7]. But, such a simulation based approach at a fundamental level has several drawbacks. Another proposed solution is the use of programmable logic devices such as CPLDs or FPGAs, and the use of hardware description languages (HDLs) like VHDL or Verilog, to perform both computer simulations as well as hardware synthesis of various logic blocks involved in digital electronics experiments [8]. However, the introduction of the concepts of hardware description languages at an introductory level, usually the first or second year of an undergraduate curriculum, is not a viable solution owing to the steep learning curve of HDLs. The prohibitively high cost of CPLD or FPGA based development boards as well as the JTAG based devices required to program them are also a deterring factor in using such programmable devices at an introductory level of the curriculum. In this paper, we propose the use of the Schematic Capture utility available within the Integrated Synthesis Environment (ISE) software provided by Xilinx for the implementation of all of the features required for digital electronics experiments, previously performed using the 74 series ICs, on a low-cost CPLD based development board that we have designed. This approach not only retains the hands on laboratory experiments but also introduces the undergraduate

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students to programmable logic devices.This rest of this paper has been organized as follows: Section II provides an overview of various programmable logic devices and highlights the specific features of CPLDs that make it a suitable candidate to replace 74-series TTL Logic ICs. Section III introduces the AkshayaPatra, an indigenous low-cost CPLD Development Kit that is capable of hosting a wide range of digital electronics experiments. Section IV outlines the methodology for performing experiments using the CPLD Development Kit and compares the proposed technique to the conventional methods currently used to perform these experiments. Section V summarizes the efficacy of the proposed alternative for tackling the obsolescence of 74-series TTL ICs.

II. OVERVIEW OF PROGRAMMABLE LOGIC DEVICES

Before the advent of programmable logic devices (PLDs), arbitrary combinational logic functions with multiple inputs and outputs were implemented on Read-Only Memory (ROM) chips. The XC157, manufactured by Motorola in 1969, was the first programmable gate array with 12 mask-programmable gates and 30 input/output pins [9]. The Programmable Logic Array (PLA), developed by Texas Instruments in 1970, was capable of implementing combinational logic circuits expressed in a sum-of-products (SOP) form [10]. The Programmable Array Logic (PAL) by Monolithic Memories Inc. [11] and the Generic Array Logic (GAL) by Lattice Semiconductor [12] were among other popular techniques used for implementation of combinational logic. These devices generally are of small size, equivalent to around a few hundred logic gates.

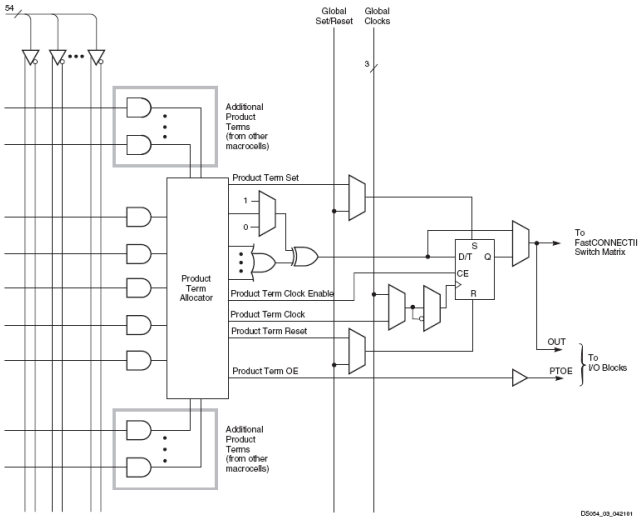

Fig. 1. Structure of a Macrocell of a Xilinx XC9500XL Family CPLD [13]

For applications that have much bigger requirements, complex programmable logic devices (CPLDs) are used. The building block in a CPLD is a macrocell, which is capable of implementing disjunctive normal form expressions as well as other specialized logic. A typical macrocell in a modern CPLD is shown in figure 1. A typical CPLD contains from tens to thousands of macrocells, each of which is equivalent to around 20-30 logic gates. For more advanced applications, such as implementations of complex state machines and processors, field programmable gate arrays (FPGAs) are used. The building block of FPGAs is a hardware lookup table (LUT) and typically an FPGA has an equivalent of tens of thousands to several million logic gates. CPLDs and FPGAs are usually programmed in-circuit using a JTAG interface.

CPLDs and FPGAs are increasingly being used as single chip replacements for applications that traditionally required the use of a large number of discrete logic ICs. This makes them excellent candidates for use in digital electronics laboratories where the obsolescence of the 74 series TTL ICs are becoming a matter of immediate concern. In the recent times, the high cost of these programmable logic devices and the complexities involved in programming them for simple applications have acted as a deterrent in their adoption for use in fundamental digital electronics laboratories. While the use of schematic capture tools in design synthesis, as proposed in this paper, reduces the complexity in implementation of digital logic, the cost of hardware is still high. Commonly available experimentation platforms that use CPLDs – such as CoolRunner range from Xilinx, Cyclone and Max family from Altera or the Mach series from Lattice Semiconductor – are prohibitively expensive solutions [14]. While some relatively low cost CPLD solutions exist [15], they require an expensive external JTAG adapter for programming.

III. THE AKSHAYAPATRA PLATFORM

AkshayaPatra, derived from the Sanskrit word meaning 'inexhaustible vessel', is an low cost CPLD development platform built around the Xilinx XC9572XL CPLD, designed and developed at the Centre for Electronics Design and Technology, Netaji Subhas Institute of Technology, New Delhi. AkshayaPatra, depicted in figure 2, is an easy to use experimentation platform, targeted for use in fundamental as well as intermediate level digital electronics laboratories. The CPLD on board is programmed using a JTAG bridge implemented on a very low-cost microcontroller, reducing the overall bill of materials cost of the AkshayaPatra platform.

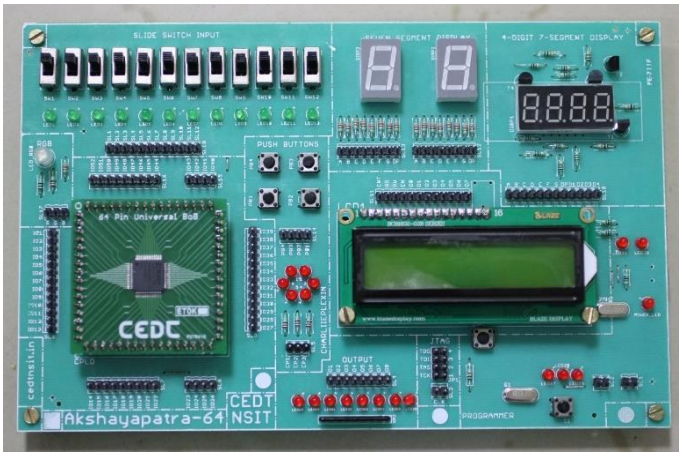

Fig. 2. The AkshayaPatra CPLD Development Board

A. Features of AkshayaPatra

The AkshayaPatra is a digital electronics experimentation platform with a host of peripherals that can be interfaced to the programmable logic device on board. The peripherals have been chosen for their utility in performing basic digital electronics experiments, which have been traditionally performed using 74 series ICs, either connected on a breadboard, or using a commercially available laboratory trainer kit.

The list of peripherals on board the AkshayaPatra is as follows:

- 12 Toggle Switch Inputs with Indicator LEDs
- 4 Tactile Push Button Switches
- 8 Individual Output LEDs
- 1 RGB LED
- 6 LEDs connected in a Charlieplexing configuration
- 2 Single Digit Seven Segment Displays
- 1 Four Digit Multiplexed Seven Segment Display
- 1 16x2 Character LCD

Unlike commonly available CPLD development boards, none of the peripherals are directly connected to the input/output pins of the on-board CPLD. Instead, the connections to each of the peripherals are made available on pin headers, which can be connected to any available I/O pin of the CPLD using an appropriate jumper wire. As opposed to the pre-committed connections to peripherals on existing CPLD boards, this un-committed configuration allows for more flexibility in the experiments that can be performed using the AkshayaPatra kit. It also gives the student a more hands-on approach to performing experiments, as it requires the student to assign appropriate I/O pins on the CPLD and also make the requisite electrical connections required for performing an experiment. The un-committed connections of the CPLD's I/O pins also allows the student to probe and observe the state of any pin on an oscilloscope or a logic analyzer.

The AkshayaPatra features a Xilinx XC9572XL High Performance CPLD operating at a system voltage of 3.3V. The input/output pins are 5V tolerant and can accept 5V, 3.3V and 2.5V logic levels. The device can operate up to a frequency of 178 MHz with pin-to-pin logic delays of 5ns. The XC9572XL has four 54-input function blocks, each with 18 macrocells, providing a total of 72 macrocells with 1600 usable gates on chip, and 34 to 72 I/O pins depending on the device package [16].

The XC9572XL is programmed using the on-chip Full IEEE Standard 1149.1 compliant JTAG controller, and has an endurance rating exceeding 10,000 program/erase cycles [x]. The AkshayaPatra implements a JTAG bridge on a low-cost microcontroller, which communicated with the host computer using a USB-UART link. The Integrated Synthesis Environment (ISE) software provided by Xilinx is capable of generating a binary file containing the JTAG boundary scan vectors in a proprietary serial vector format called XSVF. A user-friendly GUI (as shown in fig. 3) designed using Python that runs on the host computer is used to send the XSVF file generated by the ISE software to program the CPLD via the JTAG Bridge implemented on the on-board microcontroller.

This novel low-cost JTAG Bridge implementation results in a significant reduction in the overall bill of materials cost of the system. All the relevant hardware and software designs of the AkshayaPatra platform have been made open source, and further details regarding the platform can be obtained from the URL http://wiki.cedtnsit.in/.

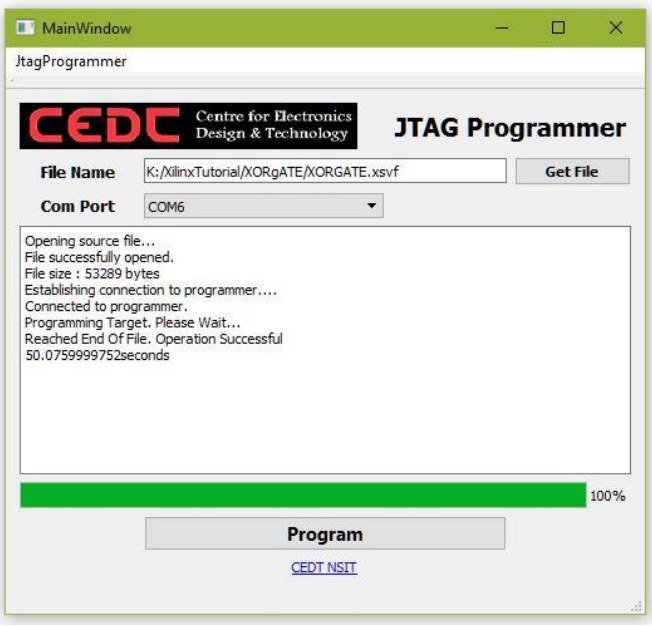

Fig. 3. GUI used for programming the CPLD using the JTAG Bridge

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IV. USING CPLDs FOR DIGITAL ELECTRONICS LABORATORY EXPERIMENTS

The AkshayaPatra CPLD development kit was used to perform several experiments prescribed in the curriculum of the introductory digital circuits and systems laboratory course of Delhi University [17]. The experiments prescribed in the curriculum that traditionally use 74 series logic ICs are as follows:

1. Implementation of Half Adder / Subtractor
2. Implementation of Full Adder / Subtractor
3. Implementation of 4-bit Binary Adder
4. Design of Adder-Subtractor using Full Adder
5. Build Flip-Flops (RS & D-Type) using NAND Gates
6. Build JK Master-Slave Flip-Flop using Flip-Flop ICs
7. Implementation of 4-bit counter
8. Implementation of 4-bit shift register

As detailed in Table 1, all the experiments listed above are well within the capabilities of the XC9572XL CPLD, utilizing no more than 10% of the available macrocells of the device and less than a third of the available I/O pins of the device. It was observed that most of the experiments in intermediate as well as advanced level digital electronics courses, such as design and implementation of arithmetic and logic unit (ALU), as well as simple experiments involving finite state machines (FSMs) are also well within the capabilities of the AkshayaPatra kit.

TABLE I. RESOURCE UTILIZATION ON XC9572XL CPLD

Experiment Name	Macro cells	Pterms	Registers	Pins	Inputs
Half Adder	2/72 (3%)	3/360 (1%)	0/72 (0%)	4/52 (8%)	4/216 (2%)
Full Adder	2/72 (3%)	6/360 (2%)	0/72 (0%)	5/52 (10%)	6/216 (3%)
Four Bit Adder	7/72 (10%)	46/360 (13%)	0/72 (0%)	14/52 (27%)	18/216 (9%)
Adder Subtractor	7/72 (10%)	58/360 (17%)	0/72 (0%)	14/52 (27%)	30/216 (14%)
RS flip flop	2/72 (3%)	5/360 (2%)	0/72 (0%)	5/52 (10%)	7/216 (4%)
D flip flop	2/72 (3%)	4/360 (2%)	0/72 (0%)	4/52 (8%)	6/216 (3%)
JK Master-slave	5/72 (7%)	8/360 (3%)	0/72 (0%)	5/52 (10%)	9/216 (5%)
4-bit Counter	4/72 (6%)	4/360 (2%)	4/72 (6%)	5/52 (10%)	4/216 (2%)
4-bit shift register	5/72 (7%)	10/360 (3%)	0/72 (0%)	4/52 (8%)	8/216 (4%)

By using the Schematic Capture utility of the Xilinx ISE software, the usual prerequisites for using programmable logic devices, such as the knowledge of hardware description languages, is eliminated. The screenshots shown in figure 4, 5, 6 and 7 illustrate the procedure for performing digital electronics experiments using the AkshayaPatra kit.

The required logic circuit is implemented as a schematic in the ISE software. Subsequently, the Pinout and Area Constraints Editor (PACE) utility is used to assign the inputs and outputs of the logic circuit implemented on to any specified pin of the CPLD. The circuit synthesis is performed using the ISE software and the iMPACT tool is used to generate the XSVF file required for programming. Finally, the python based GUI is used to program the CPLD on board the AkshayaPatra via the JTAG Bridge.

The ISim utility of the Xilinx ISE Software also allows the user to simulate the behavior of the design, as shown in figure 8 and 9. This gives the student useful information regarding the expected behavior of the implemented logic circuit, so that the results can be correlated with observations made using the hardware.

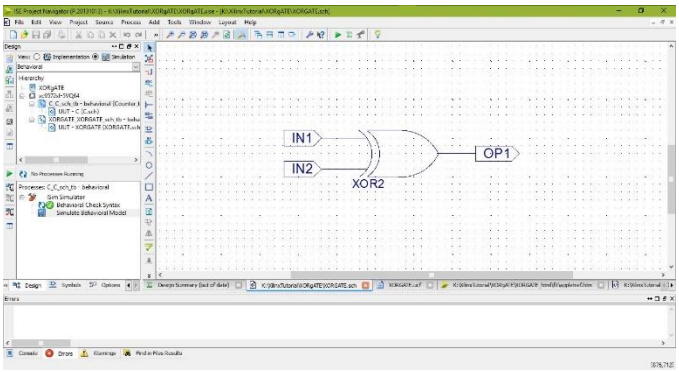

Fig. 4. XOR Gate implemented using Schematic Capture

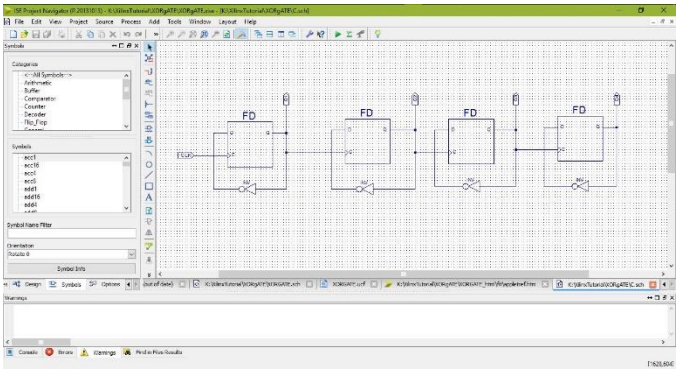

Fig. 5. 4-bit Counter implemented using Schematic Capture

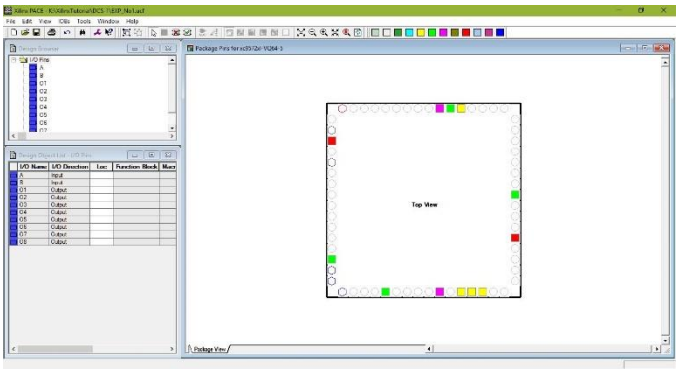

Fig. 6. Pin Assignment using the Xilinx PACE utility

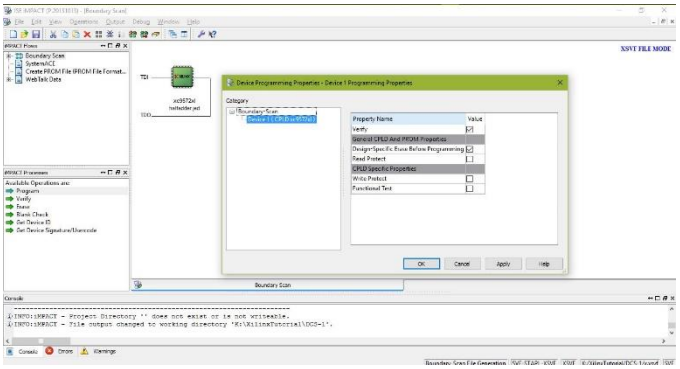

Fig. 7. XSVF File Generation using the Xilinx iMPACT utility

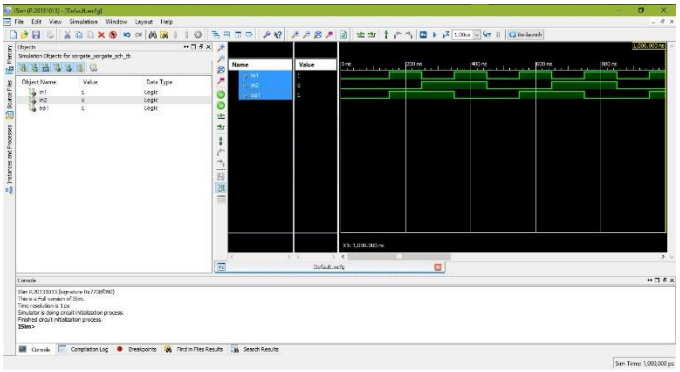

Fig. 8. Simulation of XOR Gate (fig 4) using ISim utility

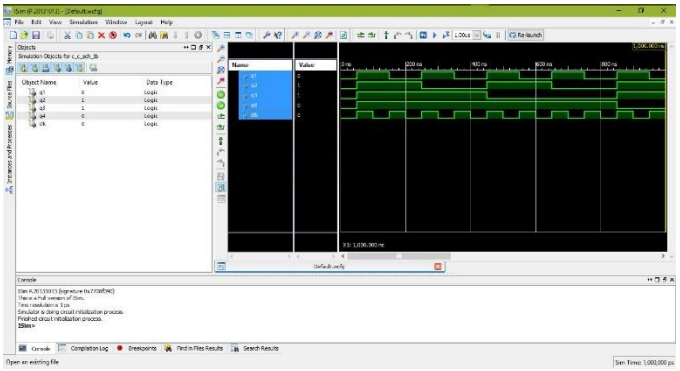

Fig. 9. Simulation of 4-bit Counter (fig. 5) using ISim utility

A side-by-side comparison of the procedure for performing introductory level digital electronics experiments using the conventional method of 74-series logic ICs as well as the proposed solution using the CPLD based experimenter board is shown in Table 2.

TABLE II. COMPARISON OF EXPERIMENTATION METHODOLOGY

Using 74-series ICs	**Using AkshayaPatra**
Using the truth table of the given logic circuit derive simplified expressions	
Draw the circuit diagram for the designed implementation	Implement the design using the schematic capture tool
Study the pinout of the 74-series logic IC and identify the pins to be used	Use the pinout editor to assign inputs and outputs in the schematic to CPLD pins
Connect the circuit on the breadboard/trainer kit	Create the XSVF file and program the CPLD
Make connections to appropriate input and output peripherals	
Perform the experiment and observe the results	

V. CONCLUSION

A CPLD based digital experiment board, with all the necessary on-board input and output peripheral devices, specially with a microcontroller based USB to JTAG bridge can provide an inexpensive solution to the impending crisis of disappearing 74 series of TTL ICs which form the bulwark of current introductory digital electronics laboratory. Use of schematic capture based entry method does not alter the current learning approach nor imposes any additional requirements of skills on the students. Incorporation of such programmable logic devices based laboratory platform at an entry level learning course also prepares and sensitizes the students to such platforms in more advanced courses albeit with hardware description language approach [18]. The only adverse impact on the laboratory logistics is the requirement of sufficient number of computer platforms to host the schematic capture and bit file download software.

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