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Course Code: MCA-107 Course Name: Computer Organization

Practice Questions (Theory)

SUBJECTIVE QUESTIONS

1. Design a typical stage that implement the following logic micro-operation
   (a)P_1: A← AV B (b)P_2: A← A ' (c)P_3: A← A^ B (d)P_4: A← A Ex-or B
2. A non-pipeline system takes 60ns to process a task. The same task can be processed in a five- segment pipeline with a clock cycle of 20 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?
3. Calculate the transfer rate of an eight-track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per inch?
4. Convert the following arithmetic expression into infix notation:
   (a) ABC*/D-EF/+
   (b) ABCDEFG+*+*+*
5. Design 16 ×1 MUX using 4×1 MUX.
6. Design SR-Flip Flop. Draw its Excitation Table & Characteristics table using NOR gate SR-F/F.
7. Design Bus system for four registers? Give its Truth Table.
8. Discuss applications of stack. Explain 64-bit word stack. Write RTL notation for Stack Operations.
9. What is two-way set-associative mapping Cache? What is write-through & write-back in Cache?
10. Draw timing diagram, Block Diagram & sequence of events of data transfer via hand shaking
11. Draw the Block diagram for the hardware that implements the following statements:
    x+yz: AR to AR+BR
12. Implement the Following Function using 8×1 MUX :
    $F(A,B,C,D)= \sum(2,3,6,7,8,9,10,11)$
    Draw the Circuit Diagram for the same.
13. Discuss one stage of Arithmetic logic shift unit.
14. What is Tri-state buffer? Draw Bus line using tri-state buffer.
15. What is the difference between access time and cycle time of a memory? Which is larger?
16. For an array multiplexer circuit that multiplies two unsigned four –bit number, Calculate the following:

(a)How many AND gates are required?
(b) How many adders and of what size is required?
(c) How many bits are there in final product?

17. Compare I/O mapped and memory mapped I/O. Give their applications.
18. How that any three variable logic function f(x, y, z) can be realized using 2-input multiplexer. Give the realization & truth table.
19. Explain the use of following registers:
(a)PC (b)MAR (c)IR (d)MDR
20. A digital system has 16 registers, each with 32 bits. it is necessary to provide parallel data transfer from each register to every other register. **7**
(a) How many lines are needed for transfer along 4 common bus?
(b) How many lines are needed for direct parallel transfer?
(c) If the registers form a scratch-pad memory, how is information transferred from one register to another? Let the register in the memory be designated as R0 TO R15.
(d) List the sequence of micro operations for a transfer of contents R6 to R13
21. Briefly describe the various categories of instructions in a general purpose microprocessor. Suppose that you have to design the instruction set architecture for a special purpose microprocessor that carries out basic graphic functions, what extra instruction(s) and register(s) would you suggest ?
22. A program contains 1000 machine instructions. These are executed in a 7 stage instruction **7** pipeline. Due to various data dependencies,10 cycles are wasted for every batch of 50 instructions. Branch instructions cause a further wastage of 20% extra cycles. Calculate the speed up of the pipeline as compared to a non-pipeline processor.
23. Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operation for evaluating the numerical result.
(3+4)[10(2+6)+8]
24. A 512-bits data packet needs to be prepared with 16-bit words, for serial asynchronous **10** communications. There is 1 start bit and 1.5 stop bits for each word. The data packet is then encapsulated with 8-bit SOH,8 bit ETX and 16 bit CRC. Calculate the total overhead (in percentage) of transferring 1000 such packets.
25. A computer system needs 2 KB of RAM,2KB of ROM and 3 I/O ports with 3 registers in each. The first 1 KB of memory space is occupied by ROM and finally the I/O port addresses. To construct this memory system 512 x 8 RAM chips are used. Show the complete map of the system.
26. Write short notes on the following:
(a) Cache memory
(b) Virtual memory
(c) Memory management hardware
(d) CACHE COHERENCE
(e) SEMAPHORE AND its TSI instructions
(f) Parallel computing

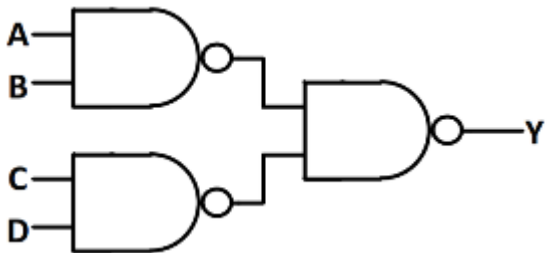
27. What are the typical applications and limitation of Relative addressing mode and Based, indexed addressing mode.
28. Define the following-Micro instruction, Micro program and Control Memory.
29. What happens when an RET instruction at the end of a subroutine is executed?
30. Design multiplexer implementations for the following functions using the numerical method. The simulation should be used to check the workings.
    $Z=f(A,B,C,D)= \Sigma(0,1,2,3,5,7,8,10,12,13,15)$.

MCQ Type Based Questions

1. When we use auto increment or auto decrements, which of the following is/are true?
   1) In both, the address is used to retrieve the operand and then the address gets altered
   2) In auto increment, the operand is retrieved first and then the address altered
   3) Both of them can be used on general purpose registers as well as memory locations
   (a) 1, 2, 3
   (b) 2
   (c) 1, 3
   (d) 2, 3
2. Which method/s of representation of numbers occupies a large amount of memory than others?
   (a) Sign-magnitude
   (b) 1's complement
   (c) 2's complement
   (d) 1's & 2's compliment
3. ____ method is used to map logical addresses of variable length onto physical memory.
   (a) Paging
   (b) Overlays
   (c) Segmentation
   (d) Paging with segmentation
4. The wrong statement/s regarding interrupts and subroutines among the following is/are _____
   i) The sub-routine and interrupts have a return statement
   ii) Both of them alter the content of the PC
   iii) Both are software oriented
   iv) Both can be initiated by the user
   (a) i, ii and iv
   (b) ii and iii
   (c) iv
   (d) iii and iv
5. The sub-routine service procedure is similar to that of the interrupt service routine in _____
   (a) Method of context switch
   (b) Returning
   (c) Process execution
   (d) Method of context switch & Process execution

6. The technique whereby the DMA controller steals the access cycles of the processor to operate is called _____
   (a) Fast conning
   (b) Memory Con
   (c) Cycle stealing
   (d) Memory stealing
7. When the processor receives the request from a device, it responds by sending _____
   (a) Acknowledge signal
   (b) BUS grant signal
   (c) Response signal
   (d) None of the mentioned
8. The Master strobes the slave at the end of each clock cycle in Synchronous BUS.
   (a) True
   (b) False
9. The bootstrap program is stored in:
   (a)RAM
   (b)EEPROM
   (c)ROM
   (d)Both b & c

10. In the logic circuit shown below, Y is:

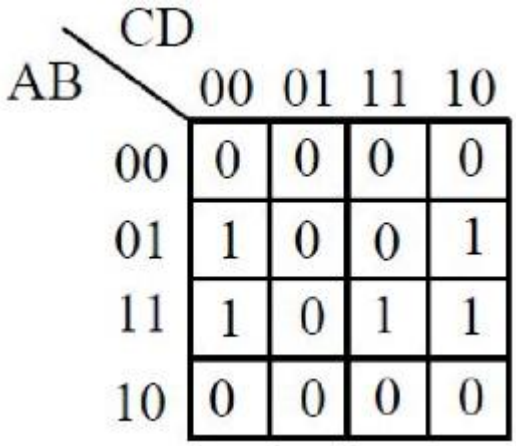
11. 

   (a)Y=ABCD
   (b)Y=(A+B)(C+D)
   (c)Y=A+B+C+D
   (d)Y=AB+CD

12. Digital input signals A,B,C with A as the MSB and C as the LSB are used to realize the Boolean function f=m0+m2+m3+m5+m7 where mi denotes the ith minterm. In addition, F has a don't care for m1. The simplified expression for F is given by
   A'C'+B'C+AC

A′+C
C′+A
A′C+BC+AC′

13. The output expression for K-map shown below is:



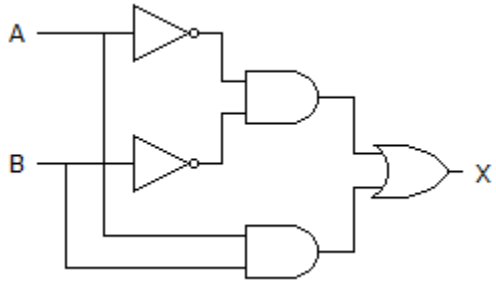
AB \ CD	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	1	1
10	0	0	0	0

(a)BD′+BCD
(b)BD′+AB
(c)B′D+ABC
(d) BD′+ABC

14. Consider the following sequence of micro-operations.
MBR ← PC
MAR ← X
PC ← Y
Memory ← MBR
Which one of the following is a possible operation performed by this sequence?
(a) Instruction fetch
(b) Operand fetch
(c) Conditional branch
(d) Initiation of interrupt service

15. The bootstrap program is stored in:
(a)RAM
(b)EEPROM
(c)ROM
(d)Both b & c

16. What type of logic circuit is represented by the figure shown below?



(a) XOR
(b) XNOR
(c) AND
(d) XAND

17. Digital input signals A,B,C with A as the MSB and C as the LSB are used to realize the Boolean function f=m0+m2+m3+m5+m7 where mi denotes the ith minterm. In addition, F has a don't care for m1. The simplified expression for F is given by

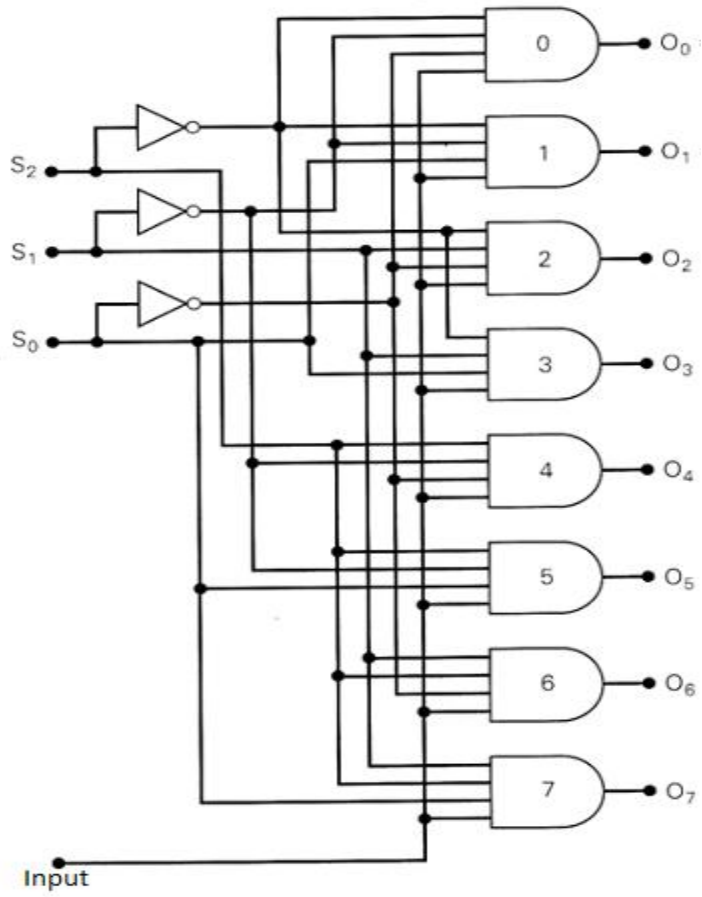
(a) A'C'+B'C+AC
(b) A'+C
(c) C'+A
(d) A'C+BC+AC'

18. The instruction fetch operation is initiated by loading the contents of program counter into the_____ and sends_____ request to memory:
(a) Memory register and read
(b) Memory register and write
(c)Data register and read
(d)Address register and read

19. In cache memory hit rate indicates:
(a) Data from requested address is not available
(b)Data from requested address is available
(c) Control from requested address is available
(d) Address from requested address is not available

20. How many RAM chips of size (256K x 1 bit) are required to build 1M Byte memory ?
(a)8
(b)12
(c)24
(d)32

21. The output Q4 of this 1-to-8 demultiplexer is _____



(a) Q2.(Q1)′.Q0.I
(b) Q2.Q1.(Q0)′.I
(c) Q2.(Q1)′.(Q0)′.I
(d) Q2.(Q1).Q0.I

22. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
(a) 0 to 2^n
(b) 0 to $2^n + 1$
(c) 0 to $2^n - 1$
(d) 0 to $2^{n+1/2}$

23. When performing subtraction by addition in the 2's-complement system _____

(a) The minuend and the subtrahend are both changed to the 2's-complement
(b) The minuend is changed to 2's-complement and the subtrahend is left in its original form
(c) The minuend is left in its original form and the subtrahend is changed to its 2's-complement
(d) The minuend and subtrahend are both left in their original form

24. Which is the most important component of a digit computer that interprets the instruction and processes the data contained in computer programs:
    (a)MU
    (b) ALU
    (c)CPU
    (d) PC

25. Which number is said to be normalized if the more significant position of the mantissa contains a non zero digit:
    (a)Binary point number
    (b) Mantissa point number
    (c) Floating point number
    (d) None of these