(Please write your Exam Roll No.) *Exam Roll No ……*

Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63
Model Question Paper-I [Sem-I]

Paper Code: MCA–107	**Subject: Computer Organization**
Time: 3 Hours	**Maximum Marks: 75**

Note: Attempt Five questions in all. Question No. 1 is compulsory and attempt one question from each unit.

1.	Answer all the following questions briefly:-		**2.5 x 10 = 25**
	(a)	Design 8*3 priority encoder.	
	(b)	Discuss the steps used by the processor for handling the interrupt ?	
	(c)	Design 16×1 MUX using 2×1 MUX.	
	(d)	List various logic micro-operations.	
	(e)	Explain Associative Memory? Discuss its read operation in detail.	
	(f)	Explain the steps of an instruction cycle.	
	(g)	Discuss the selective set and mask operation with example.	
	(h)	Draw the Block diagram for the hardware that implements the following statements: x+yz: AR AR+BR	
	(i)	A nonpipeline system takes 50 ns to process a tasks the same task can be processed with a clock cycle of 10 ns Determine the speed up ratio 100 tasks. What is the max speedup ratio that can be achieved.	
	(j)	Write RTL statement for BSA instruction..	
		UNIT - I	
2.	(a)	Design bi-directional shift register with parallel load.	**6.5**
	(b)	Design 4-bit Adder-subtractor.	**6**
3.	(a)	How many 2× 4 and 1×2 decoders are required to design 5×32 decoder. Draw the Block diagram. Include Enable.	**6**
	(b)	Implement the Following Function using 8×1 MUX : $F(A,B,C,D)= \sum(2,3,6,7,8,9,10,11)$ Draw the Circuit Diagram for the same.	**6.5**

		UNIT - II	
4.	(a)	During the execution of an Instruction, if any interrupt enters in the system, how Processor handles it. Give RTL notations associated with each phase..	**6.5**
	(b)	Discuss 7 addressing modes with examples.	**6**
5.	(a)	Explain stack operations. Discuss its operation using RTL .	**6.5**
	(b)	Discuss address sequencing of control unit.	**6**
		UNIT – III	
6.	(a)	Draw UART. Discuss its all components.	**6.5**
	(b)	Discuss Vector Processor and Array processor in detail.	**6**
7.	(a)	Explain Handshaking approach for source and destination initiated ends.	**5**
	(b)	Discuss RISC vs CISC.	**6.5**
		UNIT – IV	
8.	(a)	Discuss mapping techniques of Cache Memory.	**6.5**
	(b)	Discuss Interconnection structure of Multiprocessor.	**6**
9.		Write short notes on the following:-	
	a)	Any 2 auxiliary memory	**6**
	(b)	Virtual Memory	**6.5**