(Please write your Exam Roll No.) *Exam Roll No ……*

Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63
Model Question Paper-I [Sem-I]

Paper Code: MCA–107	**Subject: Computer Organization**
Time: 3 Hours	**Maximum Marks: 75**

Note: Attempt Five questions in all. Question No. 1 is compulsory and attempt one question from each unit.

1.	Answer all the following questions briefly:-		**2.5 x 10 = 25**
	(a)	Design Octal to Binary encoder.	
	(b)	What is Cache Memory? Discuss how one can identify different instruction format.	
	(c)	Discuss Flynn classification..	
	(d)	Write RTL statement for BSA instruction	
	(e)	Describe the mechanism of handling the interrupt generated by the processor?	
	(f)	Discuss the method of obtaining synchronization in Multiple processors?	
	(g)	What is SR-Flip Flop? Draw its Excitation Table & Characteristics table.	
	(h)	List various shift micro-operations.	
	(i)	Design8×1 MUX using 2×1 MUX.	
	(j)	What is parallel processing? How pipeline is used to achieve the same.	
		UNIT - I	
2.	(a)	Discuss one stage of Arithmetic logic shift unit.	**6.5**
	(b)	Design carry look ahead circuit.	**6**
3.	(a)	What is Tri-state buffer? Draw Bus line using tri-state buffer	**6**
	(b)	Discuss 16-bit Common Bus system. Design 4-bit arithmetic circuit.	**6.5**
		UNIT - II	
4.	(a)	Discuss applications of stack. Explain 64-bit word stack. Write RTL notation for Stack Operations.	**6.5**
	(b)	Discuss how processor handles interrupt while any instruction is executed.	**6**
5.	(a)	Explain different types of addressing mode with the help of an example?	**6.5**
	(b)	How address selection can be done using Control Memory? Discuss it.	**6**

UNIT – III			
6.	(a)	Discuss arithmetic Pipeline for floating-point addition and subtraction. Explain with the help of an example.	**6.5**
	(b)	Draw the diagram of I/O Interface. Explain the role of various registers in this interface.	**6**
7.	(a)	What is DMA Controller? Explain DMA transfer for a system.	**5**
	(b)	Draw timing diagram, Block Diagram & sequence of events of data transfer via hand shaking?	**6.5**
UNIT – IV			
8.	(a)	What is two-way set-associative mapping Cache? What is write-through & write-back in Cache?	**6.5**
	(b)	How synchronization is achieved between multiple processors?	**6**
9.	(a)	Explain mapping in segmented-page memory management unit with example.	**6.5**
	(b)	Discuss Associative Memory? Discuss its working. Also derive the equation for Match Logic used by this Memory.	**6**