(Please write your Exam Roll No.) *Exam Roll No* ……

Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63
Model Question Paper-I [Sem-I]

Paper Code: MCA–107 **Subject: Computer Organization**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt Five questions in all. Question No. 1 is compulsory and attempt one question from each unit.

1.	Answer all the following questions briefly:-		**2.5 x 10 = 25**
	(a)	Design Bus system for four registers? Give its Truth Table.	
	(b)	Explain mapping logic in Cache Memory?	
	(c)	Draw the format of various types of Instructions.	
	(d)	Discuss SISO & PIPO implementation.	
	(e)	Write RTL statement for BSA instruction.	
	(f)	How can interrupt handle by the processor?	
	(g)	How Multiple processors communicate?	
	(h)	What is SR-Flip Flop? Draw its Excitation Table & Characteristics table using NOR gate SR-F/F.	
	(i)	List various arithmetic micro-operations & shift micro-operations.	
	(j)	Design 16 ×1 MUX using 4×1 MUX	
		UNIT - I	
2.	(a)	Discuss one stage of Arithmetic logic shift unit	**6.5**
	(b)	Design carry look ahead circuit	**6**
3.	(a)	What is Tri-state buffer? Draw Bus line using tri-state buffer.	**6**
	(b)	Design 4-bit arithmetic circuit.	**6.5**
		UNIT - II	
4.	(a)	Discuss how processor handles interrupt while any instruction is executed.	**6.5**
	(b)	Convert the following arithmetic expression into infix notation: ABC*/D-EF/+ ABCDEFG+*+*+*	**6**
5.	(a)	Explain Bi-directional shift register?	**6.5**

	(b)	Design a typical stage that implement the following logic micro-operation P_1: A← AV B P_2: A← A ' P_3: A← A^ B P_4: A← A Ex-or B	**6**
		UNIT – III	
6.	(a)	A non-pipeline system takes 60ns to process a task. The same task can be processed in a five- segment pipeline with a clock cycle of 20 ns. Determine the speedup ratio of the pipeline for 120 tasks. What is the maximum speed up that can be achieved?	**6.5**
	(b)	Draw the diagram of I/O Interface. Explain the role of various registers in this interface.	**6**
7.	(a)	What are Array Processors? Explain different types of Array Processors.	**5**
	(b)	Describe the mechanism of data transfer via hand shaking. Draw timing diagram, Block diagram & sequence of events?	**6.5**
		UNIT – IV	
8.	(a)	Explain different types of mapping associated with cache memory?	**6.5**
	(b)	How synchronization is achieved between multiple processors	**6**
9.	(a)	What is Associative Memory? Discuss its working. Also derive the equation for Match Logic used by this Memory.	**6.5**
	(b)	Explain different types of interconnection structure of Multiprocessors?	**6**