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Course Code: MCA-107 Course Name: Computer Organization

Assignment 2
(Based on Unit-III)

Q 1. Consider an non-pipelined processor. Assume that it has 1-ns clock cycle and that it uses 4 cycles for ALU operations and 5 cycles for branches and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 50 %, 35 % and 15 % respectively. Suppose that due to clock skew and set up, pipelining the processor adds 0.15 ns of overhead to the clock. Ignoring any latency impact, how much speed up in the instruction execution rate will we gain from a pipeline?

Q 2. Consider the multiplication of two 40x40 matrices using a vector processor.

a) How many product terms are there in each inner product, and how many inner products must be evaluated?

b) How many multiple add operations are needed to calculate the product matrix ?

Q 3. Consider a computer with four floating point pipeline processors. Let each processor uses a cycle time of 40ns .How long will it take to perform 400 floating point operations? Is there a difference if same 400 operations are carried out using a single pipeline processor with a cycle time of 10ns?