(*Please write your Exam Roll No.*) *Exam Roll No* ……

Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63
FIRST SEMESTER [MCA] Internal Examination, September-2019

Paper Code: MCA –107	**Subject: Computer Organization**
Time: 2 Hours	**Maximum Marks: 45**

Note: Attempt THREE questions in all. Question No. 1 is compulsory and attempt one question from each unit.

1. Answer all the following questions briefly:- 1.5 x 10 = 15
   (a) Design 4-bit Shift Register performing shl and shr Register Transfer Operations.
   (b) Show the working of FGO and FGI whenever any input and output enters into the system.
   (c) Discuss RTL Notations for BSA and ISZ.
   (d) Draw the Block diagram of a dual 4*1MUX with its Function table.
   (e) Design the one stage of Logic Circuit.
   (f) Explain the terms with example:
   i)Subroutine ii)Microprogram
   (g) Generate Control Word for the following operations:
   i)ORing of R4 and R5 stored in R4
   ii)Contents of Input transfer to Output
   (h) Design 4-bit common bus system using Registers .
   (i) Values of A and B , if $(11A1B)_8 = (12c9)_{16}$ where c stands for decimal 12.
   (j) Design 6-bit Register implementing SISO operation in it.

UNIT – I

2. (a) Design 5-bit combinational circuit decrementer using full adder. 5
   (b) Show the hardware that implements the following statements: 5
   xT1+yz: A<-A+B
   where A and B are two n-bit registers and x,y,z,T1 are control variables.
   (c) Consider A=1011 and B= 1011.Design 4-bit adder–subtractor performing both operations in the same diagram. 5
3. (a) Design the following configurations: 5
   i) XOR gate using 2*1 MUX
   ii)2*4 decoder
   (b) Design the digital circuit that performs the four logic operation of XOR,NOR,NAND and XNOR. 5
   (c) An 8-bit register contains the binary value 11001010.Perform circular shift-right, followed by a logical right and a circular shift-left .Load the register with the contents 10011100. 5

UNIT - II

4. (a) A two-word instruction is stored in memory at an address register designated by the symbol A. The address field of the instruction , stored at A+1 is designated by the symbol B. The operand used during execution of the instruction is stored at an address symbolized by C. An index register contains the value α. State how C 5

is calculated from the other addresses if addressing mode of the instruction is:
i)Indexed ii)Relative iii)direct iv)Direct

(b) What is Hardwired and Microprogrammed Control Unit? Design Block diagram of Hardwired Control Unit. 5

(c) Elaborate how addresses are mapped to Control memory with required diagram. 5

5. (a) Represent the given expression in Two-address and Zero-address format: 5
X=A-B+C*(D*E)-F/G*H

(b) Discuss and Show the various steps for the identification of specific type of Instruction. Discuss RTL notations for every phase of it Also state the steps when R Flip-flop is set to 1. 5

(c) Perform the Conversion: 5
i)Infix to reverse polish notation: ((A-(B+C))*D)$(E*F)
ii) Reverse Polish Notation to Infix : ABCDE+*-/