(*Please write your Exam Roll No.*) *Exam Roll No* ……

Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63
FIRST SEMESTER [MCA] Internal Examination, October 2017

Paper Code: MCA –107	**Subject: Computer Organization**
Time: 2 Hours	**Maximum Marks: 45**

Note: Attempt FOUR questions in all. Question No. 1 is compulsory and attempt one question from each unit.

1. Answer all the following questions briefly:- 1.5 x 10 = 15
   (a) Formulate a control word for RTL as:
   R5←R5-1
   (b) Design a circuit where a single control signal can be used to control both addition and subtraction operation.
   (c) Write RTL notations for Push & Pop operation of Stack.
   (d) Brief the approaches used to design Control unit.
   (e) What is Race condition? Name the flip-flops which exhibit this condition.
   (f) Discuss any two extended applications of logic micro-operations.
   (g) Represent six-segment instruction pipeline by considering a set of instruction.
   (h) How subroutine call is different from Branching?
   (i) If DMA approach is used, Is it effective or not ? Justify your answer.
   (j) How the data dependency conflict of pipeline can be resolved? Discuss it with example.

UNIT - I

2. (a) Design 64×1 MUX using 8×1 MUX. Draw the block diagram. Show one level circuit diagram also. 5
   (b) What is the value of output Z if input A is 1101with inputs S=1,I_r=0 & I_l=1 are passed to a 4-bit shift register? Draw the respective block diagram for the same. 5

OR

3. (a) Design 4-bit arithmetic circuit of an ALU. List various operations that can be carried using the circuit. 5
   (b) Show the hardware that implements the following statement. Draw the block diagram for the **Binary counter** with a count enable input: 5
   $xyT_0+T_1+y'T_2$:AR←AR+1

   Also write down the RTL notation for BUN & BSA instruction.

UNIT - II

4. (a) Discuss the approach to identify memory reference, Input-output and register reference instruction. Write RTL notation for every phase associated with it. 5
   (b) Convert the following expression into RPN: 5
   (i) AB*C-D+E/F
   (ii) A*B+A*(B*D+C*E)

OR

(a) Discuss Eight addressing modes with an example. 5

(b) Discuss RTL notations for Instruction cycle. Also brief how an interrupt is handle by the processor? 5

UNIT - III

6. (a) How multiple interrupts are managed by the processor. Discuss the hardware approach that uses serial implementation of the circuit? 5

(b) Explain application of vector processor which uses pipeline concept. 3

(c) Give an example to show the implementation of Pipeline with Parallel processing. 2

OR

7. (a) Explain how data transmission occurs between CPU and I/O using asynchronous modes. 5

(b) Differentiate between RISC vs CISC instruction format. 2.5

(c) Brief any two types of Array processor. 2.5