

(Please write your Exam Roll No.)

Exam Roll no.

**Bharati Vidyapeeth's
Institute of Computer Applications and Management
A-4, Paschim Vihar, New Delhi-63**

MCA-01st Semester, Internal Examination, Batch: 2016-19

Paper Code: MCA 107

Subject: Computer Organization

Max. Marks: 45

Max. Time: 02 Hrs

Note: Attempt one question from each unit including Q.no.1 which is compulsory.

Q.1. Attempt any five questions: (3×5=15 Marks)

- (a) Discuss the Mapping logic used for the selection of address for control Memory.
- (b) How Branch instruction act as a conflict in Pipeline? How one can resolve the same Problem?
- (c) What is Tri-state Buffer? Design Bus line using it.
- (d) Give RTL notations for any of two memory-reference instruction.
- (e) Draw the block diagram for designing a 4-bit Bus system.
- (f) Let SP=000000 in the stack with a 64-word stack. How many items are there in the stack?

If:

- i) FULL=1 and EMPTY=0
- ii) FULL=0 and EMPTY=1

UNIT-I

- Q2 (a) How many 2× 4 and 1×2 decoders are required to design 5×32 decoder. Draw the Block diagram. Include Enable. 3
- (b) What is Priority Encoder? How 4×2 Priority Encoder works? 4
- (c) Draw the block diagram of 4-bit arithmetic circuit. 3

OR

- Q3.(a) Implement the Following Function using 8×1 MUX : 4
 $F(A,B,C,D) = \sum(2,3,6,7,8,9,10,11)$
Draw the Circuit Diagram for the same.
- (b) Discuss the Working of a 4-bit combinational circuit shifter. 3
- (c) Draw the diagram of a 6-bit Adder subtractor. Discuss role of Control signal 3

UNIT-II

- Q4. During the execution of an Instruction, if any interrupt enters in the system, how Processor handles it. Give RTL notations associated with each phase. 6

Q5 .A Computer has 16 registers, an ALU with 32 operations and a shifter with eight operations, all connected to a common bus system. 6

- a. Formulate the Control Word.
- b. Specify the number of bits in each field of the control word and give a general encoding scheme.

OR

Q6. A two word instruction is stored at an address designated by the symbol W. The Address field is designated by Y. The operand used during execution of instruction is stored At Z. An Index Register contains the value of X. Calculate the address using

- a)Direct mode 6
- b)Immediate Mode
- c) Relative
- d) Indexed

Evaluate it using Memory Component.

UNIT-III

Q7. Explain how the performance of the Instruction Pipeline can be improved. 5

Q8. Write short note on: 5

- (a) Array Process
- (b) Memory Interleaving

OR

Q9. Differentiate RISC vs. CISC. Also Discuss how memory is involved when any 5 RISC instruction gets executed.

Q10.How data can be transmitted in an Asynchronous Mode. Explain Handshaking Process With the help of the timing diagram. Write all sequence of events. 5