(Please write your Exam Roll No.) *Exam Roll no. ……*

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MCA-01st Semester , Internal Examination, Batch: 2015-18

Paper Code: MCA 107	***Subject: Computer Organization***
Max. Marks: 45	***Max. Time: 02 Hrs***
Note: Attempt one question from each unit including Q.no.1 which is compulsory.	

Q.1. Attempt any five questions: (3×5=15 Marks)

(a) Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder.
(b) Draw the Block diagram for the hardware that implements the following statements:

x+yz: AR ← AR+BR

(c) A nonpipeline system takes 50 ns to process a tasks the same task can be processed with a clock cycle of 10 ns Determine the speed up ratio 100 tasks. What is the max speedup ratio that can be achieved?
(d) Define the selective set and mask operation with example.
(e) Draw the Block and timing Diagram for destination-imitated transfer using handshaking.
(f) Discuss the race round condition in J-K flip flop.
(g) Generate a Control Word for the micro operation:
i) R4 to R4 V R5 (where OR opcode = 01010)
ii) R7 ← R1

UNIT-I

Q.2 (a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in} .Draw the logic diagram for the first two stages (7)

S	C_{in} =0	C_{in} =1
0	D=A+B(add)	D=A+1(Increment)
1	D=A-1(Decrement)	D=A+B'+1(subtract)

(b)Design 4-bit Adder-subtractor. (3)

Q.3 (a) Design bi-directional shift register with parallel load. (5)

(b)

(i) Design a 4 bit decrementer circuit using full adders. (2)

(ii) Show a typical stage of Arithmetic logic shift unit. (3)

UNIT-II

Q.4 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (5)

a. Direct
b. Immediate
c. Relative
d. Register indirect
e. Index with R1 as the index register.

or

Q.5 (a) Evaluate the following expression (5)

$$X = \frac{(A + B - (C \cdot D - F))}{(G - K \cdot H)}$$

Using

a. Three address instruction
b. Two address instruction
c. One address instruction
d. Zero address instruction.

(b) Explain Instruction cycle and Interrupt cycle with the help of flowchart. (5)

UNIT-III

Q.6. (a) Design the Circuit diagram of 4×4 FIFO Buffer. Explain its working with the help of a function Table. (5)

(b) Explain various types of conflicts associated with Pipeline. Also discuss Delayed load & Delayed branch with example. (5)

Q.7. (a) Explain the Floating point addition with the help of an example using Pipeline (5)

(b) Explain in details Daisy Chain priority interrupt Scheme. (5)

********ALL THE BEST********