(Please write your Exam Roll No.) Exam Roll No. 82585304418

END TERM EXAMINATION

FIRST SEMESTER [MCA] NOVEMBER-DECEMBER 2018

Paper Code: MCA-107 *Subject: Computer Organization*

Time: 3 Hours *Maximum Marks: 75*

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each Unit.

Q1 Answer **any ten** of the following:- **(1.5x10=15)**

(i) Differentiate between computer organization and architecture.

(ii) Represent the following conditional control statement by two register transfer statements with control functions.

if (P=1) then (R1 ← R2) *elseif* (Q = 1) then (R1← R3)

(iii) Define selective-set with example.

(iv) A digital computer has a memory unit with 24 bits per word. The instruction set consists of 190 different operations. Each instruction is stored in one word of memory and consists of an op-code part and address part. How many bits are needed for operation code and address part of an instruction?

(v) Why does the peripheral connected to computer need special links for interfacing them with CPU?

(vi) What is the difference is between isolated and memory mapped I/O?

(vii) A processor has 16 registers, an ALU with 16 logic and arithmetic functions and a shifter with 8 operations, all connected by an internal processor. Design a micro-instruction format to specify the various micro-operations for the processor.

(viii) The content for the top of stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the contents of PC, SP and top of stack after call instruction is executed?

(ix) An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in address space and memory space?

(x) Explain hand shaking process in asynchronous transmission.

(xi) Explain relevance of memory interleaving in pipelining/vector processing.

(xii) What is the purpose of snoopy controller?

UNIT-I

Q2 (a) Design 3x8 decoder using two 2x4 decoders. **(5)**

(b) Design circuit for 4 bit combinational shifter. **(5)**

(c) Consider the register transfer statements for two 4-bit registers R1 and R2.

$xT: R1 \leftarrow R1 + R2$

$x'T: R1 \leftarrow R2$

Draw the diagram showing the hardware implementation of the two statements. Use the block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2 to 1 line multiplexer that selects the input for register R1. In the diagram, show how the control variables x and T select the inputs of the multiplexer and the load input of register R1. **(5)**

P.T.O.

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OR

Q3 (a) Design a 4-bit arithmetic circuit. **(5)**

(b) Draw and discuss the functioning of Master Slave flip flop in brief. **(5)**

(c) Draw a diagram of a bus system for transfer of four register with 4 bit each using multiplexer. **(5)**

UNIT-II

Q4 (a) Evaluate X=(A+B)*(C+D) using three, two, one and zero address instruction **(10)**

(b) Design micro-program sequencer for a control memory **(5)**

OR

Q5 (a) Discuss different addressing modes with example. **(10)**

(b) Design a common bus system for basic computer with common ALU and 16 registers PC, AR, IR, TR, DR, AC, OUTR, INPR etc and memory capacity of 4096 words and each word contain 16 bits, input and output operations are performed using 8 bits. **(5)**

UNIT-III

Q6 (a) Explain four possible hardware schemes that can be used in instruction pipeline in order to minimize the performance degradation caused by instruction pipeline. **(10)**

(b) Discuss SIMD Array Processor in detail. **(5)**

OR

Q7 (a) A commercial interface unit uses different names for handshake lines associated with the transfer of data from I/O devices into interface unit. The interface input handshake line is labeled STB (strobe), and the interface output handshake line is labeled IBF (input buffer full). A low-level signal on STB loads data from the I/O bus into the interface data register. A high level signal on IBF indicates that the data item has been accepted by the interface. IBF goes low after an I/O read signal from the CPU when it reads the content of the data register.

(i) Draw a block diagram showing the CPU, the interface, and the I/O device together with the pertinent interconnection among the three units. **(5)**

(ii) Obtain a sequence-of-events flowchart for the transfer from the device to the interface and from the interface to the CPU **(5)**

(b) Design parallel priority interrupt hardware for a system with eight interrupt sources. **(5)**

UNIT-IV

Q8 (a) Discuss different interconnection structure between components of multiprocessor system. **(10)**

(b) An address space is specified by 24 bits and the corresponding memory space by 16 bits. **(5)**

(i) How many words are there in address space?

(ii) How many words are there in memory space?

(iii) If a page consists of 2K words, how many pages and blocks are there in the systems?

OR

Q9 (a) Discuss different mapping scheme between main and cache memories. **(10)**

(b) Write short notes on Memory management hardware **(5)**

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