(Please write your Exam Roll No.)

Exam Roll No. 08

END TERM EXAMINATION

FIRST SEMESTER [MCA] DECEMBER 2016

Paper Code: MCA-107 **Subject: Computer Organization**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt any five questions including Q.no.1 which is compulsory.

Q1 Answer **any Ten** of the following: **(2.5x10=25)**

(a) What is De-Multiplexer? How can you make decoder to function as a Demultiplexer? Show this by a block diagram and truth table?

(b) Assume a 4 bit arithmetic circuit is enclosed in one IC package. Show the connections among two such IC's to form an 8 bit arithmetic circuit.

(c) Why data bus is bidirectional and address bus is unidirectional in most microprocessor? Justify.

(d) Define selective compliment with example.

(e) Give an example that uses delayed load with the three-segment pipeline.

(f) Explain operand forwarding.

(g) Write symbolic micro-program routine for BSA.

(h) Why does the peripheral connected to computer need special links for interfacing them with CPU?

(i) Explain hand shaking process in asynchronous transmission.

(j) Assume that the three output xyz from the priority encoder are used to provide a vector address of the form 101xyz00. List the eight vector addresses starting from the one with the highest priority.

(k) It is necessary to transfer 256 words from a magnetic dist to memory section starting from address 1230. The transfer is by means of DMA, give the initial value that the CPU must transfer to the DMA controller.

(l) Explain relevance of memory interleaving in pipeline/vector processing.

(m) An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in address and memory space?

(n) What is the purpose of snoopy controller?

Q2 (a) Construct a full adder using 3-to-8 decoder with enable. **(6.25)**

(b) Design a 4-bit combinational circular shifter circuit. **(6.25)**

Q3 (a) Consider the register transfer statements for two 4-bit registers R1 and R2.

$$xT: R1 \leftarrow R1 + R2$$
$$x'T: R1 \leftarrow R2$$

Draw the diagram showing the hardware implementation of the two statements. Use the block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2 to 1 line multiplexer that selects the input for register R1. In the diagram, show how the control variables x and T select the input of the multiplexer and the load input of register R1. **(6.25)**

(b) Design a 4-bit arithmetic circuit. **(6.25)**

Q4 (a) The content of PC in the basic computer is 3AF. The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. (The hex code for Add is 1xxx and 9xxx for direct and indirect addressing mode respectively). **(4)**

(i) What is the instruction that will be fetched and executed next?

(ii) Show the operation that will be performed in the AC when the instruction is executed.

P.T.O.

MCA-107

P.1/2

(iii) Give the content of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and sequence counter SC in the binary at the end of the instruction cycle.

(b) Draw a flowchart for computer operation. **(8.5)**

Q5 (a) Design a bus organization for seven CPU register and common ALU. **(6.25)**

(b) Design the system for selection of address for control memory of 1024 words of 32 bits each. The microinstruction format is of three fields. The micro-operation has 16 bits. Also specify the following in the diagram: **(6.25)**

(i) How many bits are there in the branch address and select field.

(ii) If there are 16 bits in the system, how many bits of the branch logic are used to select a status bit?

(iii) How many bits are left to select an input for the multiplexer?

Q6 (a) Design daisy chain priority interrupt for three devices, along with one stage of the daisy chain priority arrangement. **(6.25)**

(b) Design the 4 segment arithmetic pipeline for floating point addition for addition and subtraction. **(6.25)**

Q7 (a) Suppose that we want to perform the combined multiply and add operation with a stream of numbers

$$Ai * Bi + Ci \quad for \quad i = 0 \text{ to } 7$$

Each sub operation is to be implemented in a segment within a pipeline. Each segment has one or two register and a combinational circuit. The pipeline has the following propagation times: 40 ns for the operand to be read from memory into registers R1 and R2, 45 ns for the signal to propagate through the multiplier, 5 ns for the transfer into R3 and 15 ns to add the two numbers into R5. **(5.5)**

(i) What is the minimum clock cycle time that can be used?

(ii) A non-pipeline system can perform that same operation by removing R3 and R4. How long will it take to multiply and add the operands without suing the pipeline?

(iii) Calculate the speedup of the pipeline for 10 tasks.

(iv) What is the maximum speedup that can be achieved?

(b) Discuss difference modes of data transfer to and from peripherals. **(7)**

Q8 (a) A computer system needs 2 KB of RAM, 2 KB of ROM and 3 I/O ports with 3 registers in each. The first 1 KB of memory space is occupied by ROM and finally the I/O port addresses. To construct this memory system 512 x 8 RAM chips are used. Show the complete memory map of the system. **(6.25)**

(b) Write short notes on **any one**: **(6.25)**

(i) Virtual memory

(ii) Memory management hardware

Q9 (a) Construct a diagram for 4x4 omega switching network. Show the switch setting required to connect input 3 to output 1. **(6.25)**

(b) Main memory M1 and disk memory M2 constitute two level hierarchy virtual memory system that contains page frames as follows;

M1 page frame: a, b, c

M2 page frame: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

The CPU is generating page request in a sequence as 0, 1, 2, 4, 2, 3, 7, 2, 1, 3 and 1 by employing LRU, OPT and FIFO page replacement policies, find out the following(s). **(6.25)**

(i) The hit ratio for each policy

(ii) The one which produces best results.

****

MCA-107