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Course Code: MCA-107 Course Name: Computer Organization

Class Test 1

Time: 1 Hour Max Marks: 20

Each Question carries 2 marks

1. Digital input signals A,B,C with A as the MSB and C as the LSB are used to realize the Boolean function f=m0+m2+m3+m5+m7 where mi denotes the i^{th} minterm. In addition, F has a don't care for m1. The simplified expression for F is given by

(a) A'C'+B'C+AC
(b) A'+C
(c) C'+A
(d) A'C+BC+AC'

2. The output expression for K-map shown below is:

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	1	1
10	0	0	0	0

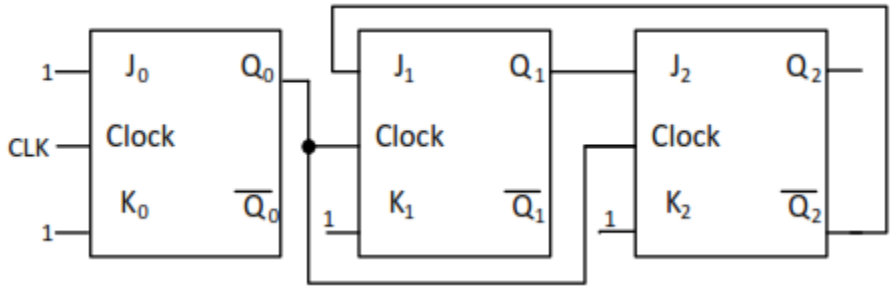
(a)BD'+BCD

(b)BD'+AB

(c)B'D+ABC

(d) BD'+ABC

3. The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of Q2Q1Q0=000. This state Q2Q1Q0=000 will repeat after _____ number of cycles of the clock CLK.



(a)5
(b)6
(c)10
(d)7

4. f(A, ,B, C, D)=∏M(0,1,3,4,5,7,9,11,12,13,14,15) is a maxterm representation of a Boolean function f(A,,B,C,D) where A is the MSB and D is the LSB. The equivalent minimized representation of this function is

(a) (A+C'+D)(A'+B+D)
(b) AC'D+A'BD
(c) A'CD+AB'CD'+AB' C'D'
(d) (B+C'+D)(A+B'+C'+D)(A'+B+C+D)

5. Procedure for the design of combinational circuits are:
A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
C. Simplify the switching expression(s) for the output(s).
D. Implement the simplified expression using logic gates.
E. Write down the switching expression(s) for the output(s).
(a) B, C, D, E, A
(b) A, D, E, B, C
(c) A, B, E, C, D
(d) B, A, E, C, D

6. 3 bits full adder contains _____
(a) 3 combinational inputs
(b) 4 combinational inputs

(c) 6 combinational inputs
(d) 8 combinational inputs

7. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
(a) 3
(b) 4
(c) 2
(d) 5

8. The characteristic equation of S-R latch is _____
(a) Q(n+1) = (S + Q(n))R′
(b) Q(n+1) = SR + Q(n)R
(c) Q(n+1) = S′R + Q(n)R
(d) Q(n+1) = S′R + Q'(n)R

9. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____
(a) 01110
(b) 00001
(c) 00101
(d) 00110

10. A three digit decimal number requires _____ for representation in the conventional BCD format.
(a) 3 bits
(b) 6 bits
(c) 12 bits
(d) 24 bits