Laboratory Manual

(Version 10.0)

for

Computer Organization Lab

(MCA-155)

MCA - I Semester

Compiled by:

Mrs. Manu Anand

(Assistant Professor, BVICAM, New Delhi)

Bharati Vidyapeeth's
Institute of Computer Applications and Management (BVICAM)

A-4, Paschim Vihar, Rohtak Road, New Delhi-63

Visit us at: www.bvicam.in

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List of Abbreviations

BTL	Bloom's Taxonomy Level
CE	Communication Efficacy
CICP	Conduct Investigations of Complex Computing Problems
CK	Computational Knowledge
CO	Course Outcome
DAC	Departmental Advisory Committee
DDS	Design and Development of Solutions
I&E	Innovation and Entrepreneurship
I&T	Individual & Team Work
IQAC	Internal Quality Assurance Cell
LLL	Life-Long Learning
MTU	Modern Tool Usage
PA	Problem Analysis
PE	Professional Ethics
PEO	Programme Educational Objective
PMF	Project Management and Finance
PO	Programme Outcome
SEC	Societal and Envoirnmental Concern

Declaration

Department	:	Department of Computer Science and Applications
Course, Year and the Semester to which Lab is offered	:	MCA - I Year, I Semester
Name of the Lab Course	:	Computer Organization Lab
Course Code	:	MCA-155
Version No.	:	10.0
Name of Course/Lab Teacher	:	Mrs. Manu Anand
Laboratory Manual Committee	:	1. Mrs. Vaishali Joshi, Chairperson 2. Dr. Anupam Baliyan, Member 3. Dr. Ritika Wason, Member 4. Mrs. Tanya Pathak Garg, Member 5. Mr. Uttam Singh Bist, Member 6. Prof. P. S. Grover, Margdarshak 7. Mr. Amit Sharma, Alumni & Industry Expert 8. Dr. Ritika Wason, Concerned Subject Teacher, Convener
Approved by	:	DAC Date: 03/05/2019
Approved by	:	IQAC Date: 04/05/2019

Signature (Course Teacher)	**Signature** (Head of Department)	**Signature** (IQAC Coordinator)

1. Vision of the Department

To become a Centre of excellence in the field of Computer Science and Applications, to contribute effectively in the rapidly changing global economy directed towards national development ensuring prosperity for the mankind.

2. Mission of the Department

M1 To become a centre of excellence in the field of Computer Science and Applications and produce professionals as per global industry standards.

M2 To foster innovation, entrepreneurial skills, research capabilities and bring all-round development amongst budding professionals.

M3 To promote analytical and collaborative life-long learning skills, among students and faculty members involving all stakeholders.

M4 To inculcate strong ethical values and professional behaviour while giving equal emphasis to social commitment and nation building.

3. Programme Educational Objectives (PEOs)

The PEO's for the MCA programme are as follows:

PEO1 Exhibit professional competencies and knowledge for being a successful technocrat.

PEO2 Adopt creative and innovative practices to solve real-life complex problems.

PEO3 Be a lifelong learner and contribute effectively to the betterment of the society.

PEO4 Be effective and inspiring leader for fellow professionals and face the challenges of the rapidly changing multi-dimensional, contemporary world.

4. Programme Objectives (POs)

PO1: Computational Knowledge (CK)

Demonstrate competencies in fundamentals of computing, computing specialisation, mathematics, and domain knowledge suitable for the computing specialisation to the abstraction and conceptualisation of computing models from defined problems and requirements.

PO2: Problem Analysis (PA)

Identify, formulate, and analyze complex real-life problems in order to arrive at computationally viable conclusions using fundamentals of mathematics, computer sciences, management and relevant domain disciplines.

PO3: Design and Development of Solutions (DDS)

Design efficient solutions for complex, real-world problems to design systems, components or processes that meet the specifications with suitable consideration to public health, and safety, cultural, societal, and environmental considerations.

PO4: Conduct Investigations of Complex Computing Problems (CICP)

Ability to research, analyze and investigate complex computing problems through design of experiments, analysis and interpretation of data, and synthesis of the information to arrive at valid conclusions.

PO5: Modern Tool Usage (MTU)

Create, select, adapt and apply appropriate technologies and tools to a wide range of computational activities while understanding their limitations.

PO6: Professional Ethics (PE)

Ability to perform professional practices in an ethical way, keeping in mind cyber regulations & laws, responsibilities, and norms of professional computing practices.

PO7: Life-Long Learning (LLL)

Ability to engage in independent learning for continuous self-development

as a computing professional.

PO8: Project Management and Finance (PMF)

Ability to apply knowledge and understanding of the computing and management principles and apply these to one's own work, as a member and leader in a team, to manage projects in multidisciplinary environments.

PO9: Communication Efficacy (CE)

Ability to effectively communicate with the technical community, and with society at large, about complex computing activities by being able to understand and write effective reports, design documentation, make effective presentations, with the capability of giving and taking clear instructions.

PO10: Societal and Envoirnmental Concern (SEC)

Ability to recognize and assess societal, environmental, health, safety, legal, and cultural issues within local and global contexts, and the consequential responsibilities applicable to professional computing practices.

PO11: Individual & Team Work (I&T)

Ability to work in multi-disciplinary team collaboration both as a member and leader as per need.

PO12: Innovation and Entrepreneurship (I&E)

Ability to apply innovation to track a suitable opportunity to create value and wealth for the betterment of the individual and society at large.

5. Institutional Policy for Students' Conduct

The following guidelines shall be followed:-

5.1 All the students in their introductory Lab. shall be assigned a system, which shall be their workplace for the complete semester. Students can store records of all their Lab. assignments on their individual workstations.

5.2 Introductory Lab. shall include an introduction to the appropriate software/tool, followed by a basic Introductory Assignment having Practice

Questions. All the students are expected to complete this assignment within a week time, as the same shall be assessed through a lab. test.

5.3 Each week the instructor, in parallel to respective topics covered in the theory lecture, shall assign a set of practical problems to the students in form of Assignments (A, B, C, ...). The problems in these assignments shall be divided into two parts. The first set of Problems shall be compulsory for all the students and its record need to be maintained in the Prcatical File, having prescribed format, as given in Appendix-A. All the students should get the weekly assigntment checked and signed in the Practical File by the respective teacher in the immediate succeeding week. The second set of problems are Advanced Problems and shall be optional. Student may solve these advanced problems for their further practice.

5.4 Cellular phones, pagers, CD players, radios and similar devices are prohibited in the classrooms, laboratories and examination halls.

5.5 Laptop-size computers / Tablets may be used in lectures for the purpose of taking notes or working on team-projects.

5.6 The internal practical exam shall be conducted towards the end of the semester and shall include the complete set of Lab exercises conducted as syllabus. However, students shall be assessed on continuos basis through overall performances in regular lab. tests, both announced and surprise and viva-voce.

5.7 The respective faculty shall prepare and submit sufficient number of practical sets of computing problems to the Dean (Examinations), atleast two weeks prior to the actual exam. It is the responsibility of the faculty to ensure that a set should not be repeated for more than 5 students in a given batch.

5.8 The exam shall be of 3 hours duration where the student shall be expected to implement solutions to his/her assigned set of problems on appropriate software tools in the lab.

5.9 Once implemented, student shall also appropriately document code implemented in the assigned answer sheets, which shall be submitted at the

end of the examination. All the students shall also appear for viva-voce examination during the exam.

5.10 Co-operate, Collaborate and Explore for the best individual learning outcomes but copying or entering into the act of plagiarism is strictly prohibited.

6. Learning Outcomes of Laboratory Work

The student shall demonstrate the ability to:

- ☑ Verify and Implement the concepts and theory learnt in class.
- ☑ Code and use Software Tools to solve problems and present their optimal solutions.
- ☑ Apply numerical/statistical formulas for solving problems/questions.
- ☑ Develop and apply critical thinking skills.
- ☑ Design and present Lab as well as project reports.
- ☑ Apply appropriate methods for the analysis of raw data.
- ☑ Perform logical troubleshooting as and when required.
- ☑ Work effectively as a member of a team in varying roles as need be.
- ☑ Communicate effectively, both oral and written.
- ☑ Cultivate ethics, social empathy, creativity and entrepreneurial mindset.

7. Course/Lab Outcomes (COs)

CO1 Are you able to work with digital kit and logism simulator. (BTL 6)

CO2 Are you able to Implement complex combinational and sequential circuits using both digital kit and logism simulator. (BTL 3)

CO3 Are you able to Troubleshoot complex circuits using both digital kit and logism simulator. (BTL 6)

CO4 Implement arithmetic, shift and logic microoperations using digital kit/simulator. (BTL 3)

CO5 Translate digital logic aspects into real world circuits like Traffic Light simulator and LED lights. (BTL 2)

8. Mapping of COs with POs

Table 1: Mapping of COs with POs

PO/CO	PO_1	PO_2	PO_3	PO_4	PO_5	PO_6	PO_7	PO_8	PO_9	PO_{10}	PO_{11}	PO_{12}
CO_1	3	-	-	-	3	3	2	-	-	3	-	-
CO_2	3	3	2	-	-	-	3	-	-	3	-	-
CO_3	3	3	3	-	2	-	-	-	2	2	-	-
CO_4	3	3	3	-	3	-	2	-	-	2	-	-
	3	3	3	-	-	3	-	-	-	3	3	2

9. Course/Lab Description

Course (Lab) Title	:	Computer Organization Lab
Course (Lab) Code	:	MCA-155
Credits	:	01
Pre-requisites	:	Basics of Digital Electronics
Academic Session	:	July to December
Contact Hours/Week	:	02 (01 Labs of 02 hours each/Week)
Internal Assessment	:	40 Marks
External Assessment	:	60 Marks

10. Grading Policy

Item	Points	Marks	Remarks
Weekly Lab Assignments including Practical Files	10	10	Closed Book/Open Book

Item	Points	Marks	Remarks
Internal End-Term Practical Examination	20	10	Closed Book
Viva-Voce	20	10	Closed Book
External End-Term Examinations	60	60	Closed Book (conducted and evaluated by the University)
	Total	**100**	

11. Lesson Plan

Week No.	Lab No.	Topics / Concepts to be Covered	Reference of Lab Manual
1.	1.	Familiarize with IC Chips, Connecting Wires and Digital Kit. Demonstration of IC chips working on Digital Kit. Identification and Verification of various IC chips on Digital Kit. Implement and Verify Basic Circuits using logic gates.	Assignment A (Problem AP1 To AP5)
2.	2.	Implementation and Verification of Basic Combinational Circuits.	Assignment B (Problem BP1 To BP6)
3.	3.	Designing and Verification of Larger Size Combinational Circuit using smaller size C.C.	Assignment B (Problem BA1 To BA3)
4.	4.	Learn to handle Multiple Inputs for given Combinational circuits on Digital Kit and Logism.	Assignment B (Problem BA4 To BA5)
5.	5.	Implementation and Verification of Basic Sequential Circuits.	Assignment C (Problem CP1 To CP4)
6.	6.	Designing and Verification of other components of system using combinational circuit & sequential circuit.	Assignment C (Problem CA1 To CA3)
7.	7.	Buffer Reserved for Revision	Assignment C

Week No.	Lab No.	Topics / Concepts to be Covered	Reference of Lab Manual
8.	8.	Designing and Verification of Arithmetic Circuit of system.	Assignment D (Problem DP2)
9.	9.	Designing and Verification of Logic Circuit of system.	Assignment D (Problem DP1)
10.	10.	Buffer Reserved for Revision	Assignment D (Problem DA1,DA2)
11.	11.	Designing and Verification of Shift circuit of system.	Assignment D (Problem DP3)
12.	12.	Learn to handle and Design any no. of bits for complex circuits like ALU, Tri-state buffer etc.	Assignment D (Problem DA3,DA4)
13.	13.	Buffer Reserved for Revision	Assignment D

12. Assignments

Assignment Set: A

Objectives of the Assignment:

- Familiarize with IC Chips, Connecting Wires and Digital Kit.
- Demonstration of IC chips working on Digital Kit.
- Identification and Verification of various IC chips on Digital Kit.
- Implement and Verify Basic Circuits using logic gates.

CO/BTLCovered: CO1 & CO3/BTL5 & BTL6

Problems:

AP1 Identification and Verification of AND, OR, NOT, NAND, NOR and XOR gates on Digital Kit.

AP2 Design the following Circuit on Digital Kit and Logism mentioned below:

a) Universal gates using basic gates.

b) Basic gates using Universal gates.

AP3 Design and Verify De Morgan's Law on Digital Kit and Logism.

AP4 Implement and Verify the Circuit on Digital Kit and Logism for the Boolean Expression mentioned Below: ABC+C'D

AP5 Reduce the Given Expression using K-Map and Verfy the Circuit using Digital Kit and Logism:A'B'C'+A'BC'+AB'C'+AB'C'+AB'C+ABC'+ABC

Assignment Set: B

Objectives of the Assignment:

- Implementation and Verification of Basic Combinational Circuits.
- Designing and Verification of Larger Size Combinational Circuit using smaller size C.C.

  Learn to handle Multiple Inputs for given circuits on Digital Kit and Logism.

CO/BTLCovered: CO1 , CO2 & CO3 /BTL5 & BTL6

Problems:

BP1 Design and Verify half adder and full Adder.

BP2 Design and Verify half subtractor and Full subtractor.

BP3 Design and Verify 4x1 Multiplexer.

BP4 Design and Verify 1x4 Demultiplexer.

BP5 Design and Verify 2x4 Decoder.

BP6 Design and Verify 8x3 Encoder.

Advance Problems:

BA1 Design and Verify full adder using two half adders with one OR gate.

BA2 Design and Verify 16x1 Multiplexer using 8x1 Multiplexer.

BA3 Design and Verify Binary Decoder.

BA4 Design and Verify 8x3 Priority Encoder.

BA5 Design and Verify 4-bit adder Subtractor.

***Assignment Set*: C**

Objectives of the Assignment:

- Implementation and Verification of Basic Sequential Circuits.
- Designing and Verification of other components of system using combinational circuit & sequential circuit.

CO/BTLCovered: CO1 , CO2 & CO3 /BTL5 & BTL6

Problems:

CP1 Design and verify SR Latch and SR flip-flop using NAND and NOR both.

CP2 Design and verify D flip-flop

CP3 Design and verify JK flip-flop

CP4 Design and verify T flip-flop

Advanced Questions:

CA1 Design and verify master slave flip-flop

CA2 Design and Verify 2-bit Register using D-flip flop.

CA3 Design and Verify 1-bit bus system using D-flip flop.

***Assignment Set*: D**

Objectives of the Assignment:

- Designing and Verification of Arithmetic Circuit, Logic Circuit and Shift circuit of system.
- Learn to handle and Design any no. of bits for complex circuits like ALU, Tri-state buffer etc.

CO/BTLCovered: CO1 , CO2 , CO3 & CO4 /BTL5 & BTL6

Problems:

DP1 Design and Verify working of basic logic microoperations.

DP2 Design and Verify one level of arithmetic circuit using Multiplexer and Half adder.

DP3 Design and Verify 4-bit combinational circuit shifter.

Advanced Problems

DA1 Design and Verify Bidirectional shift register.

DA2 Design and Verify one stage of ALU.

DA3 Design and Verify 4-bit Arithmetic Circuit.

DA4 Design Tri-state Buffer.

APPENDIX-A

Template for the Index of Lab File

WEEK NO.	PROBLEMS WITH DESCRPTION		PAGE NO.	SIGNATURE OF THE TEACHER WITH DATE
1	AP_1			
	AP_2			
	AP_3			
2	AA_1			
	AA_2			
	AA_3			
3	BP_1			
	BP_2			
	BP_3			
	BP_4			

Note: The students should use Header and Footer mentioning their roll no. & name in header and page no. in footer

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