

# Low Power High Speed Current Conveyor based Current Comparator, Mirror Circuit and Encoder used in ADCs

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**Abstract**— This paper presents a flash ADC (Analog to Digital Converter) modules comprising of Current Mirror Circuit, Comparator Circuit and Encoder Circuit. A CCII network and positive feedback properties based novel approach of designing Current Comparator Circuit has been employed, which gives reduction in response time and hence increases the bandwidth. This makes the structure suitable for wide band applications. The circuit has been simulated using the PSPICE simulator for 180nm CMOS technology with 1.8V supply to get satisfactory output.

**Keywords**—*Pipelined ADC, simultaneous ADC, Flash ADC, Current Comparator, and Current Conveyor (CCII).*

## I. INTRODUCTION

Analog current mode techniques are widely used in analog IC design due to high speed, low power application in VLSI CMOS technologies. Most of the physical variables are analogue in nature which can take on any value in continuous range of values e.g. temperature, audio signals, speed. Hence, the systems are design for interfacing real world signals (analogue signals) with the digital ones. The digital circuits have many advantages over the analog signals namely robustness, noise immunity, low bandwidth, easily encrypted, secure, low cost etc. [1]. The circuit which is used to convert analog signal (continuous) into digital (discrete), is called an ADC (Analog to Digital Converter). It is a mixed signal device that provides an output that represents input voltage or current level. ADC provides the link between analog world of transducer and digital world of signal processing. ADCs are used in microprocessors as the same can perform processing in digitized signals. Also used in audio-video signal processing circuits, digital voltmeters, thermocouple, cell phones etc [2]. There are different types of ADC architectures, each having its own merit and demerits, namely, Dual slope A/D converter, Successive approximation A/D converter, Flash A/D converter (parallel type), Delta Sigma A/D converter.

This paper gives the circuit description of Flash ADC (also called a Simultaneous Converter or Parallel Comparator type ADC). It has highest speed among all ADCs architectures, but requires much more circuitry than other types which limits its

resolution. The basic architecture of Parallel-Comparator type ADC is shown in figure 1. Architecture of Flash ADC consists of three sections- current generator circuit, comparator circuit and an encoder. The fundamental structure consist of  $K$  comparators and a  $(K \times n)$  encoder (where  $K = 2^n - 1$ ,  $n$  being the desired resolution) [3]. There is no requirement of a clock signal as it is a one step process and no timing sequence is required.

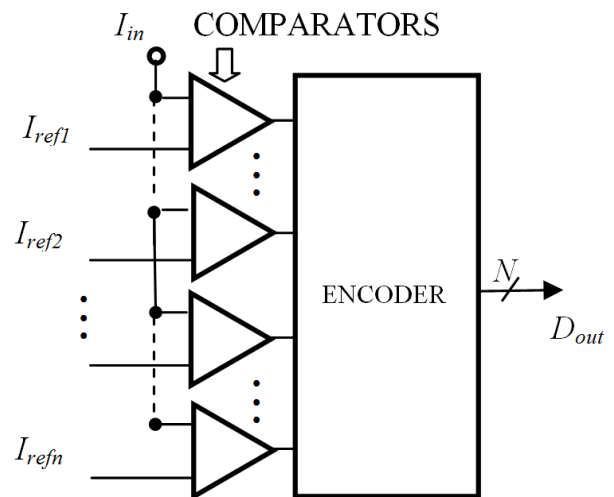


Fig. 1. Parallel-Comparator type (Flash) ADC

## II. CIRCUIT DESCRIPTION

The Flash ADC requires two currents at the input, one being the input current ( $I_{in}$ ) to be digitized and other being a set of references ( $I_{ref}$ ), one each for the current comparators, to be compared with the input current. For a 2-bit Flash ADC,  $2^2 - 1 = 3$  current comparators are required and hence 3 reference currents need to be generated. The values of reference currents are computed as follows:

If input current,  $I_{in}$ , is in the range  $(I_1 - I_2)$ , then a step  $\Delta$  is calculated as:

$$\Delta = \frac{I_2 - I_1}{2^n - 1} \quad (1)$$

Then, reference currents are computed as

$$I_{refi} = \Delta \cdot i \quad (2)$$

(where  $i = 1, 2, \dots, 2^{n-1}$ ).

Each of the current comparator compares  $I_{in}$  with a designated value of  $I_{ref}$ , as computed in (1) and produces an output 0 or 1 based on the magnitude of  $I_{in} - I_{refi}$ . This constitutes a code called thermometer code. In the next step, this thermometer code is converted into the corresponding binary code using a suitably sized Thermometer to binary encoder.

Current mirror is the basic building block of many VLSI structures used for analog and mixed mode designs. The characteristics of current mirrors decide the performance of these VLSI designs. Different types of current mirrors are presented in many research papers that are based on different characteristics used for different applications. The direction of the current that would be input to current mirror is to low impedance port while the scaled current will be to high impedance port. However the direction of current can be interchanged according to the need. The application of Current mirrors is to be used as either active load or as biasing networks. However for better insensitivity to the variations in power supply current mirrors are used in biasing networks. Temperature is also another parameter for application of insensitivity for variations.

Many comparator circuits are designed each having its own operation applications. The simplest and high speed structure is presented by Traff in 1992. However some more power efficient, speedy structures are also presented at later stage. In this paper one of the advanced architecture of comparator is concerted.

The architecture of proposed ADC, as shown in figure 2, consists of three sections, as stated above. The 1<sup>st</sup> section consists of the combination of current mirror circuit that provides differenced output current to produce the input signal at three stages. This structure is based on the difference between input current ( $I_{in}$ ) and the reference current ( $I_{ref}$ ) [3]. The output current of this stage is fed to input of comparator circuit. The comparator circuit compares the input current with internal current to produce the voltage at output. The output of the comparator circuit is transferred to the encoder circuit to produce the digital output that is desired. Each part is discussed below separately:

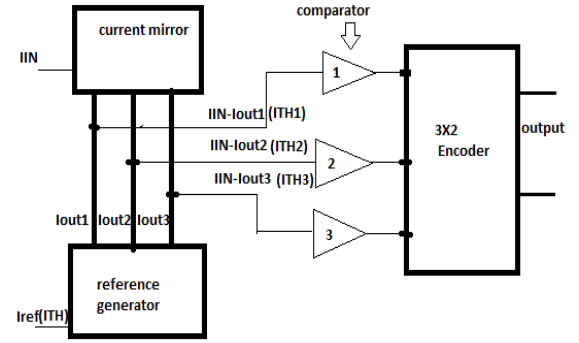


Fig. 2. Proposed Flash ADC module

#### A. Mirror circuit

As the input current  $I_{IN}$  is to be compared with  $I_{ref}$  by each of the current comparators, it is required to generate replicas of  $I_{IN}$  and progressively increasing values of  $I_{ref}$  as per (1). This is achieved by employing current mirrors. The basic current mirror circuit consists of two matched back to back MOS Transistors, such that they have same gate to source voltage, shown in figure 3. Transistor **Mn1** is enhancement type MOS. As  $V_{gs1} = V_{gs2}$  and  $V_{gd} = 0$ , the transistor **Mn1** in saturation mode. The drain of **Mn2** is connected to load circuit. The load circuit typically involves more additional stages of MOSFETs [3]. When the transistor **Mn2** is in saturation the circuit will act as current mirror (DC current source). The current **I** always goes into **Mn2** transistor, such that the circuit act as sink circuit [6].

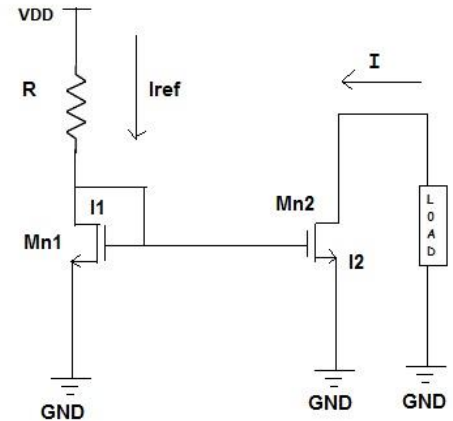


Fig. 3. Current mirror circuit

Our implementation of 2-bit ADC requires  $I_{in}$  and three values of  $I_{ref}$  to be compared to  $I_{in}$ . This is achieved with the help of a current mirror trio circuit as shown in Fig. 4. In

this circuit input current,  $I_{in}$  is applied to drain of transistor **Mn1** that is copied to **Mn2** transistor. There is combination of transistors **Mp1** and **Mn5** to provide DC reference current that is copied to **Mp2** transistor that is compared with  $I_{in}$  [3].

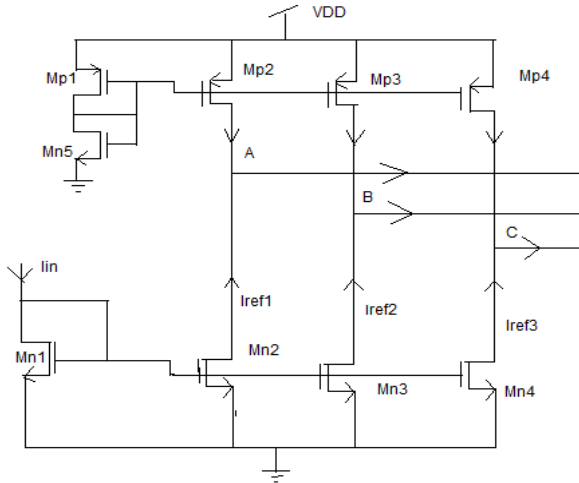


Fig. 4. Trio circuit for current mirror

We have to force  $V_{DS}$  to low so that gate will be turn off. Aspect ratio of transistor plays important role here. By varying the aspect ratios of transistors of Mp2, Mp3, Mp4 different ratio of reference current ( $I_{ref}$ ) can be obtained that is provided by the NMOS transistors.[4-5]

#### B. Current Comparator

The current comparison is based on circuital laws, which state that around a closed path, the integral of the magnetizing force is equal to the sum of the currents linked with that particular path. There should be low input impedance, low power dissipation and short propagation delay for efficient structure design. The current comparator circuits are the basic building block in non linear analog signal processing circuits and A/D converter. The main function of current comparator circuit is to distinguish the two currents and provide the output either positive or negative in digital form. The ideal current comparator has zero delay, infinite trans-impedance in transition region and zero offset. Many comparator circuits are designed each having its own operation applications.[7]-[11] However, there is still scope for improved and more efficient structures satisfying the basic performance criteria expected out of a current comparator.

We have employed a CCII (current conveyor) based current comparator (a 3 terminal analogue device) which has the ability to perform many signal processing operations, in a similar manner to the way Opamp.[6,12,13] There are many current conveyor structures are implemented, the basic structure has three nodes X,Y,Z. the input is applied to Y terminal, the same is appear at X terminal, infinite input impedance at Y terminal, with no current flows into y terminal, the voltage that is appeared at X terminal is copied to

Z terminal. There will be voltage follower at Y terminal and current follower at Z terminal.[1,14] The ideal structure of current conveyor (CCII) is shown below in figure 5.[15]-[16]

$$I_Y = I_X \quad (3)$$

$$V_X = V_Y \quad (4)$$

$$I_Z = \pm I_X \quad (5)$$

Ideally at X terminal input impedance should be low (0), and at Y and Z terminal it should be infinite, for non ideal circuit it has current gain( $\alpha(s)$ ) and voltage gain ( $\beta(s)$ ).

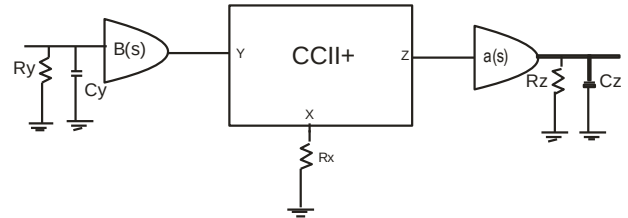


Fig. 5. Practical current conveyor circuit(CCII)

Matrix representation of same is given below. The modular diagram of CCII based comparator is shown below, figure 6.

$$\begin{bmatrix} I_X \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} \frac{1}{R_Y \parallel C_Y} & 0 & 0 \\ \beta(s) & R_X & 0 \\ 0 & \pm\alpha(s) & \frac{1}{R_Z \parallel C_Z} \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (6)$$

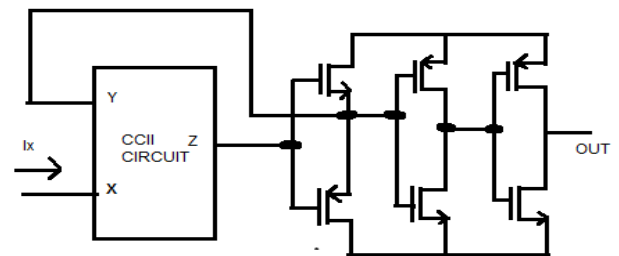


Fig 6. CCII based Current Comparator

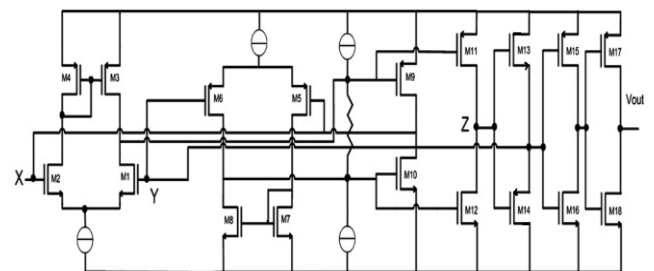


Fig. 7. Single input current comparator

### C. Encoder

The results of current comparison need to be encoded to produce the binary code at the output. A basic encoder has  $2^n$  input lines and only 1 of which is activated at a time and produces an n bit output code, depending on which input is activated. With general diagram of encoder as shown in figure 7, there are M inputs and N outputs. For our 2-bit ADC, there are 3 comparators whose outputs are to be encoded to produce a 2-bit binary output. Hence, we employ a simple 3X2 CMOS encoder. The truth table for this encoder is shown below in Table 1. The MOS circuit is given below in figure 8, having 12 transistors, however the circuit is also designed using Pass Transistor Logic. The expressions for output currents are as follows:

$$Y_0 = I_2 + I_3 \quad (7)$$

$$Y_1 = I_1 + I_3 \quad (8)$$

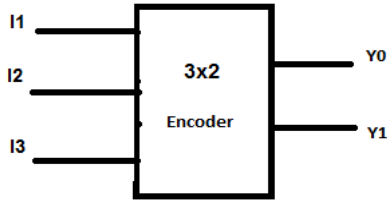


Fig. 8. 3X2 Encoder

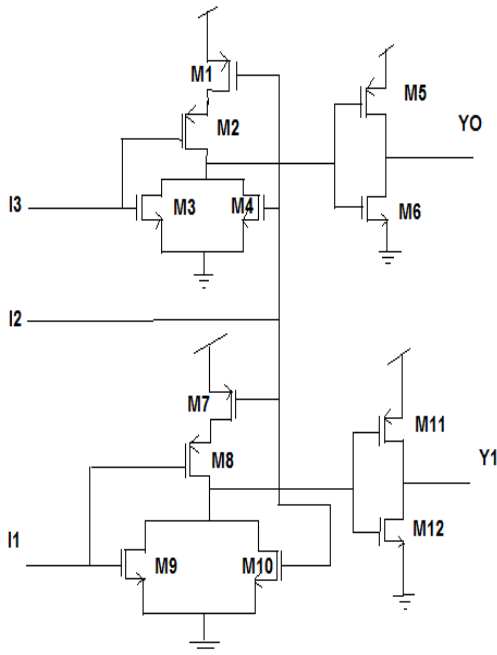


Fig. 9. Encoder (MOS Design)

TABLE I. TRUTH TABLE OF 3X2 ENCODER

| Inputs |       |       |       | Outputs |       |
|--------|-------|-------|-------|---------|-------|
| $I_0$  | $I_1$ | $I_2$ | $I_3$ | $Y_0$   | $Y_1$ |
| 0      | 1     | 0     | 0     | 0       | 1     |
| 0      | 0     | 1     | 0     | 1       | 0     |
| 0      | 0     | 0     | 1     | 1       | 1     |

### III. SIMULATION RESULTS

The structure of proposed flash ADC shown in figure 2(basic modular structure of Flash ADC) comprises of figure 4(current mirror), 7 (CCII based current comparator) and 9(encoder) has been simulated. The proposed Flash ADC's components are simulated using Pspice simulator for 0.18 $\mu$ m technology and 1.8V supply voltage.

The mirror circuit provides the different output values of current based on the different W/L ratios that is subtraction of  $I_{in} - I_{ref}$ , for providing an input signal for comparator. The range of comparator is 20uA, which means the comparator is active high after 20uA. Hence the input to the comparator that is generated by current mirror circuit is such that current up to 20uA is treated as logic 0 and above 20uA as logic 1. The output from comparator circuit provides two levels 0 and 1.8V treated as logic 0 and logic 1 as shown in simulation results.

The output from comparator circuit is fed to the Encoder to provide the output result based on the input signal. The comparator circuit provides the low power consumption and low power supply in comparison to previous comparator circuits. The propagation delay of the comparator circuit reduced to 0.5ns in comparison to Traff comparator circuit's and Tang comparator circuit's 10 and 11 nsec respectively. The power consumption is also reduced from previous comparator circuits. The output shows the good response for all circuits to provide the low power circuit designing constraint.

The circuit of encoder is simulated for three cases, ignoring the case in which we get both outputs as 0 logic as stated in truth table of 3X2 encoder, also shows satisfactory response.

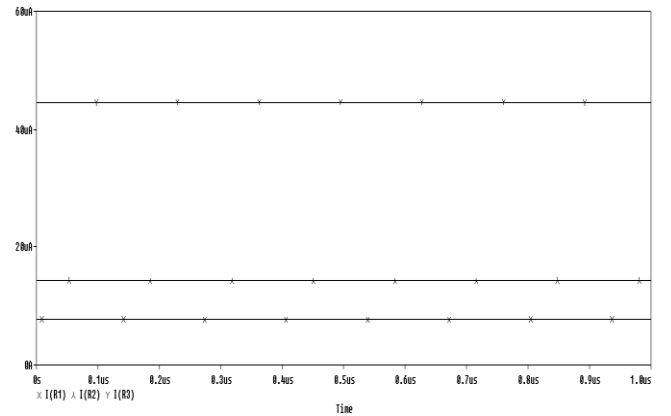


Fig. 10. Current mirror output for 001 case

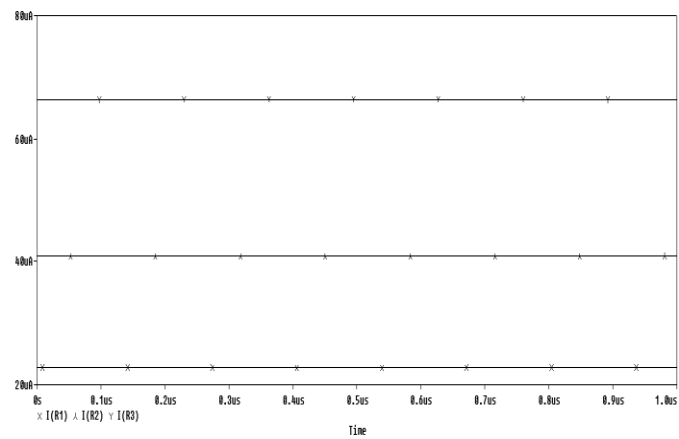


Fig. 11. Current mirror output for 111 case

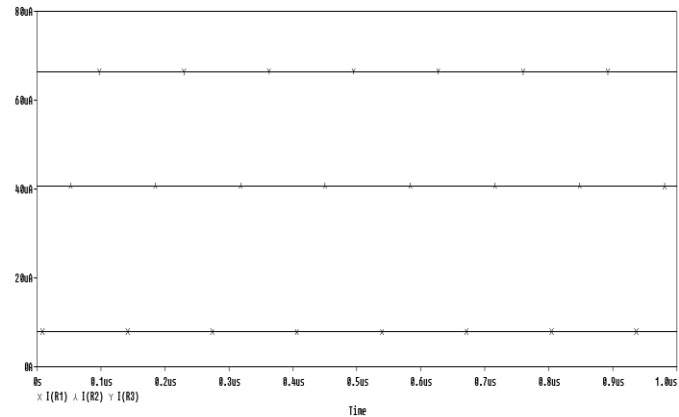


Fig. 12. Current mirror output for 011 case

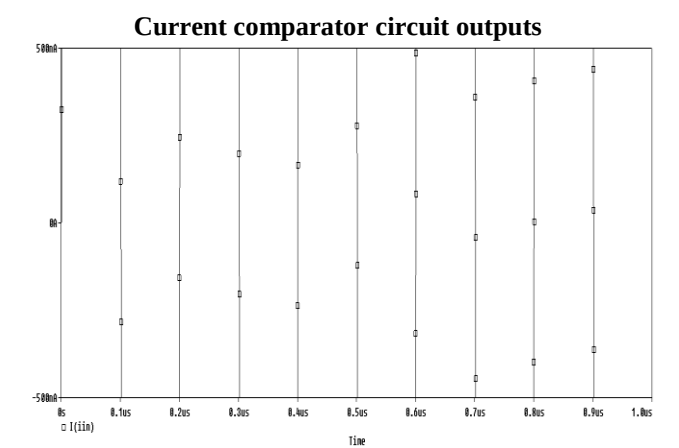


Fig. 13. Input current for current comparator circuit

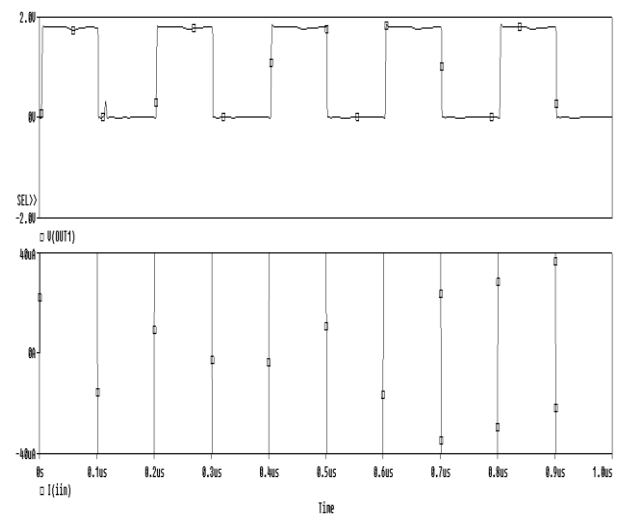


Fig. 14. Output voltage for input current  $I_{in}$

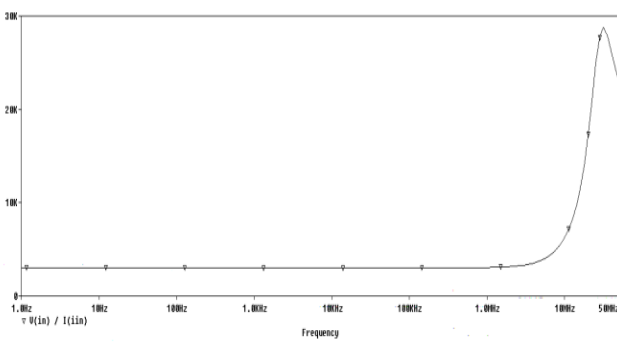


Fig. 15. Input resistance of current comparator

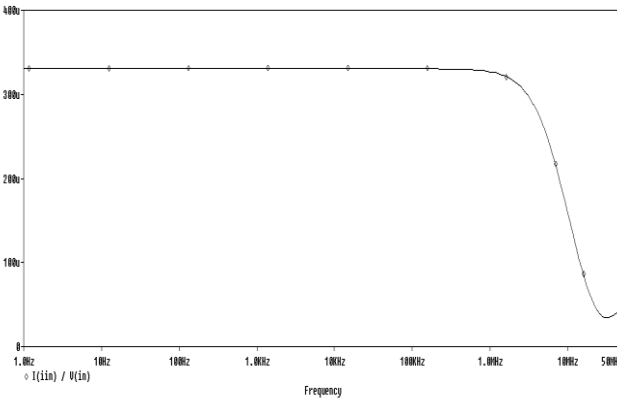


Fig. 16. Input trans-conductance of comparator

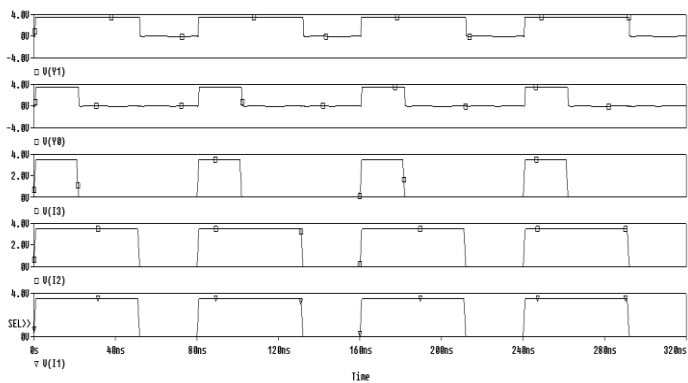


Fig. 17. Encoder Output

#### IV. CONCLUSION AND FUTURE SCOPE

The comparator circuits for high speed ADCs have been investigated. Optimization of the designs is primarily done for low propagation time, minimal input resolution and minimal circuit area. The comparator circuit topology with CC II circuit has been implemented, propagation time is reduced and power consumption is also reduced. The power consumption is reduced to about 200uW and propagation delay is about 0.9 ns. The mirror trio circuit also implemented to provide the input signal to comparator circuit, which provides the excellent response. The scalability of this ADC design in terms of applicability to newer CMOS technologies using current conveyor increases the speed and decreasing power dissipation.

The circuit modules presented in this paper used for designing different ADC structure for high speed, low power consumption namely flash ADC, Algorithmic ADC, folding and complementing structure of ADC's. However the encoder circuit MOS design concept used in this paper can be change with pass transistor logic to increase the speed more. The ADCs can be ported to even smaller CMOS technologies to achieve even higher speed. For example the PMOS transistors are replaced by the resistors, the circuit operation is possible with lower supply voltage.

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