Performance Analysis of Variation in Power Consumption and Frequency on Different Topologies of Ring VCO in 70 nm CMOS Technology

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Abstract - ***The proposed work describes the performance evaluation of different types of ring oscillator Voltage Controlled Oscillator topologies on the basis of two characteristic parameters power and frequency in 70 nm CMOS technology. The various topologies analyzed include Current Starved VCO, VCO with Gates of PMOS Transistor Grounded, VCO with PMOS Diode Connected, VCO with NMOS Diode Connected, VCO with voltage applied to both PMOS and NMOS Transistor. Simulation of different parameters of ring oscillator VCO is carried out on Tanner tool Version 13. VCO topologies are evaluated on the basis of frequency and power consumption by taking lower supply voltage of 1.2 V. Performance evaluation and comparison of different topologies results in minimum power consumption of 0.57 uW by Current Starved VCO topology and maximum operating frequency of 0.57 MHz by VCO with Gates of PMOS Transistor Grounded.***

Index Terms - Current Starved VCO, VCO With Gates of PMOS Transistors Grounded, VCO With PMOS Transistors Diode Connected,VCO With NMOS Transistors Diode Connected, VCO With Voltage Applied To Both PMOS And NMOS Transistors

1. INTRODUCTION

An oscillator that can be tuned over a wide range of frequencies by applying a voltage (tuning voltage) to it, or in other words, an oscillator that changes its frequency according to a control voltage feed to its control input is Voltage Controlled Oscillator [1]. As shown in Figure 1, the frequency of oscillation is varied by the applied controlled voltage, while modulating signals may also be fed into the VCO to cause frequency modulation (FM) or phase modulation (PM)[2][24]; a VCO with digital pulse output may similarly have its repetition rate (FSK, PSK) or pulse width modulation (PWM). The oscillator first convert voltage signal to current, and then current is converted into frequency [1]. This has numerous applications ranging from frequency synthesizers to transceivers. The design of high performance monolithic VCO has been one of the active area of research and development in recent years[22]. A CMOS VCO can be built using ring topology, relaxation circuits or LC tuned circuit [2]. The equation (1) shows the basic definition of VCO according to its operation forming a characteristic between input voltage and frequency.

$$W_{out} = W_o + K_{vco} * V_{control} \cdots\cdots\cdots \quad (1)$$

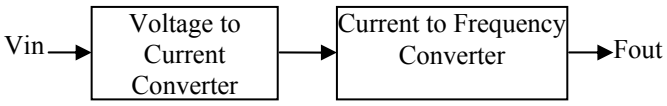

Figure 1: "Definition of VCO"

Here, W_o represents the intercept corresponding to $V_{control} = 0$ and K_{vco} denotes the 'gain' and 'sensitivity' of the circuit [2]. There are basically two types of Harmonic oscillators, LC and Ring Oscillator. The main advantage of Ring oscillator over LC oscillator is that the ring oscillator can be easily fabricated in CMOS technology as compared to LC oscillator, since the fabrication of inductor need huge amount of space [5][24].

2. DEVELOPMENT OF NEW DESIGN METHODOLOGY FOR OPTIMIZATION OF POWER WITH LOW VOLTAGE

The general source of dissipation in any CMOS circuit is the current drawn while switching. Since knowing the number and capacitance, the voltage change on a gate capacitance requires charge transfer and hence causes power consumption. Once this gate capacitance is charged, the gate can maintain the DC voltage level without any additional charge movement and does not consume any current. The required charge to change voltage levels on the gate is described by the following equation [18][24].

$$Qgate = Cgate\ V_{dd} \quad (2)$$

Qgate is the charge required to change state, Cgate is the gate capacitance, V_{dd} is the power supply voltage. Switching generates a current proportional to operating frequency (F) of the VCO. Since current is defined in terms of coulombs per second (amperes), the current can be calculated as shown in equation (4) [19].

$$I = Qgate \times Frequency = (Cgate \times V_{dd}) \times F \quad (3)$$

Where I is the current in amperes (coulombs per second)
The total current can be generalized into a figure which will include all the node capacitances in the device.

$$Idevice = Ctotal \times V_{dd} \times Fosc \quad (4)$$

where

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Idevice is the total device current,
Ctotal is the total node capacitance of all internal switching nodes,
Fosc is the switching frequency of the circuit.
All of the internal switching nodes are an unmanageable task; the current under different conditions can be determined empirically by measuring the current level for a particular known frequency and supply voltage conditions, and then scaling the current value to determine the behavior under different conditions [23]. The dependency of these currents is directly on the system operation and the supply levels [25].
The VCO power dissipation is function of its frequency hence should be modeled with care.
Average Power Dissipation = $Fosc.N.C.V_{dd}$ (5)
Here Fosc is the oscillaton frequency, C is the device capacitance and N may be the number of stages in case of a ring oscillator.
Assuming the inverters are identical, the oscillation frequency is given in equation below,

$$f_{osc} = 1/(n^* (t_{phl} + t_{plh})) \quad (6)$$

Where n is the number of inverters in the ring oscillator and $(t_{phl} + t_{plh})$ is the propagationdelay time of each inverter. The propagation delay times t_{phl} and t_{plh} determine the input to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively
Ring oscillator is designed by using five CMOS inverters having

$$(W/L)p=12/2 \text{ and } (W/L)n=5/2. \quad (7)$$

These specifications are chosen in the relation

$$(W/L)p=2.5\ (W/L)n \quad (8)$$

by applying condition for symmetric inverter i.e. $K_n=K_p$. By taking these values of W/L, if the DC characteristics of CMOS inverter are observed switching point is found to closer to $2.5(V_{dd}/2=5/2)$.
The performance evaluation and comparison on the basis of two critical parameters, power consumption and frequency, of following topologies of ring type VCOs are discussed in the proposed work [24].

- Current Starved VCO
- VCO with gates of PMOS transistors grounded
- VCO with PMOS transistors diode connected
- VCO with source voltage applied to both PMOS and NMOS transistors
- VCO with NMOS transistors diode connected

In the further sections, proposed circuit schematic of the particular topology of ring oscillator, the associated simulation results and then the tabular representation of the input parameters control voltage and time, over which the parameters under consideration, power dissipation and frequency are calculated, and the respective voltage verses frequency graphs are drawn, which are discussed individually at length.

3. CURRENT STARVED VCO

Figure 2 depicts the proposed current starved VCO. It consists of five stage ring oscillator with a current mirror circuit. This ring oscillator is designed by taking into consideration odd number of inverters which form a closed loop with positive feedback. Transistor M5 and M6 form a current mirror circuit. PMOS transistor M3 and NMOS transistor M2 form an inverter while transistors M1 and M4 are used for biasing.

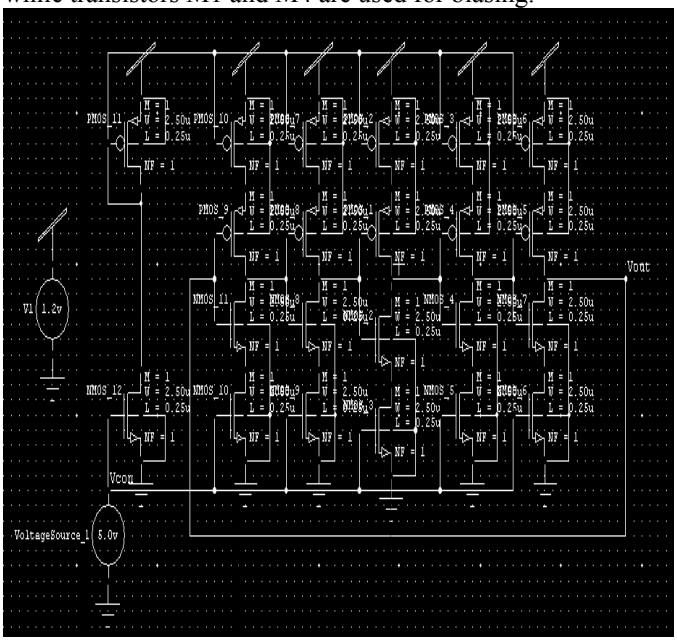


Figure 2: "Schematic circuit of Current Starved VCO"

3.1 Simulation Results:

Equation (1) defines the VCO in terms of control voltage and output frequency. This definition can be further developed for specific types of VCOs. For example equation (9) gives the output frequency of a current starved based stage selectable VCO [21].

$$f_{osc} = \beta\{ [(V_{con} - V_{ss}) - V_t][V_{DD} - V_{ss} - V_{gsp}]\}/N. C_{tot}. V_{DD} \text{ [9]}$$

Where f_{osc} is the output frequency generated by the VCO, β is the transconductance parameter, Vcon is the control voltage VDD & VSS are the power supplies, N is the number of stages, Ctot is the total capacitance on drains of MOSFETs and V_{gsp} is gate to source voltage of PMOS.
The current starved VCO circuit, performed after the transient analysis of current starved VCO with pulse input voltage, simulated using Tanner EDA ver. 13 T-spice simulator as shown in the figure 2. The number of stages of ring oscillator was optimized with center frequency of 380 Mhz. The current starved VCO draws 100uA drain current from supply voltage of 1.2V.

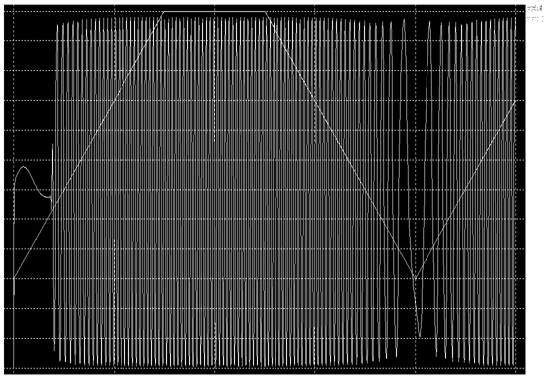


Figure 3: "Simulation results of proposed current starved VCO"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.1	500	.011	0.0006
2.	0.2	16.66	0.06	0.01
3.	0.3	7.1	0.14	0.053
4.	0.4	4.8	0.21	0.14
5.	0.5	3.70	0.27	0.28
6.	0.6	2.63	0.38	0.57
7.	0.7	2.0	0.5	1.3
8.	0.8	1.92	0.52	1.4
9.	0.9	1.92	0.52	1.5
10.	1.0	1.88	0.53	2.23
11.	1.1	1.85	0.54	2.76
12.	1.2	1.85	0.54	3.2

Table 1: "Frequency & Dynamic Power Dissipation of Current Starved VCO"

A graph is plotted between voltage and frequency as shown in the Figure 4, in order to observe the relation between these two quantities.

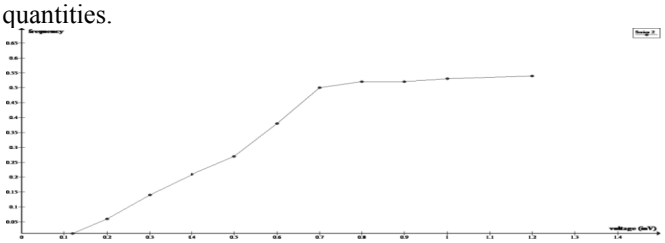


Figure 4: "Voltage vs. Frequency Plot of Current Starved VCO"

4. VCO WITH GATES OF PMOS TRANSISTORS GROUNDED

Figure 5 depicts the proposed VCO with gates of PMOS transistors grounded. It consists of five stage ring oscillator. This ring oscillator made by odd number of inverters which forms a closed loop with positive feedback.In this type of VCO, PMOS transistor is always ON since the gate terminal of PMOS transistor is connected to ground and PMOS transistor gives strong 1, so it behaves as a resistor.

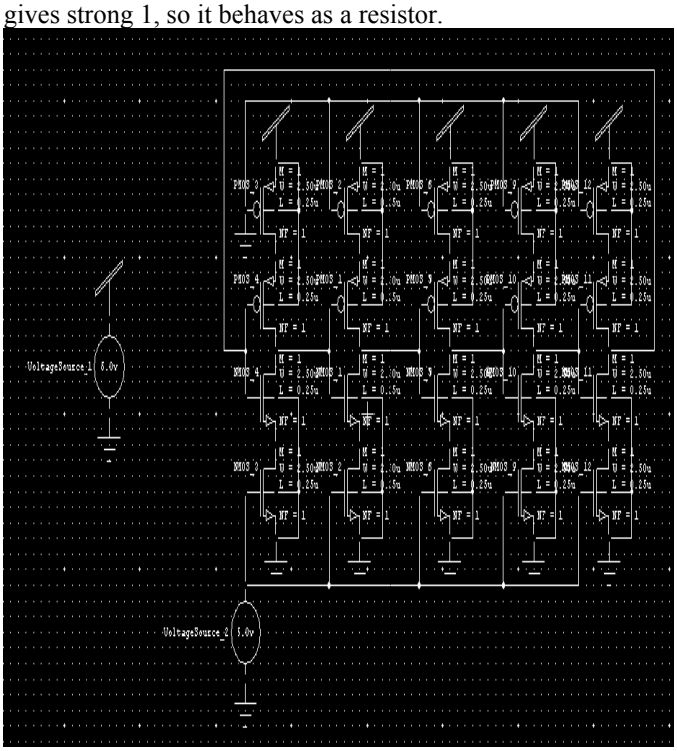


Figure 5: "Schematic Circuit of proposed VCO with gates of PMOS Transistors Grounded"

4.1 Simulation Results

The VCO with gates if PMOS transistors grounded performed after the transient analysis of PMOS transistor grounded with pulse input voltage, simulated using Tanner EDA ver. 13 simulator is as shown in the following Figure 5. The number of stages of ring oscillator was optimized with a center frequency of 470MHz. The VCO with gates of PMOS transistors grounded draws 100uA of drain current from a supply voltage of 1.2V.

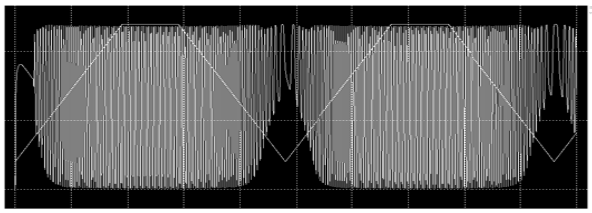


Figure 6: "Simulated results of proposed VCO with Gates of PMOS Transistor Grounded"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic Power Dissipation (uW)
1	0.1	100	0.01	0.0004
2	0.2	16.12	0.062	0.01
3	0.3	4.54	0.22	0.08
4	0.4	2.56	0.39	0.26
5	0.5	2.55	0.392	0.41
6	0.6	2.12	0.47	0.6
7	0.7	2.0	0.5	1.03
8	0.8	2.0	0.5	1.35
9	0.9	1.87	0.55	1.88
10	1.0	1.87	0.55	2.22
11	1.1	1.78	0.56	2.86
12	1.2	1.75	0.57	3.46

Table 2: "Frequency & Dynamic Power Dissipation of VCO with Gates of PMOS Transistor Grounded"

A graph is plotted between voltage and frequency, which is shown in the Figure 7, in order to observe the relation between these two quantities.

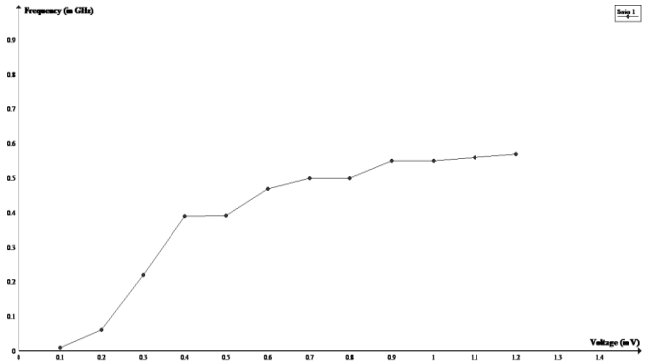


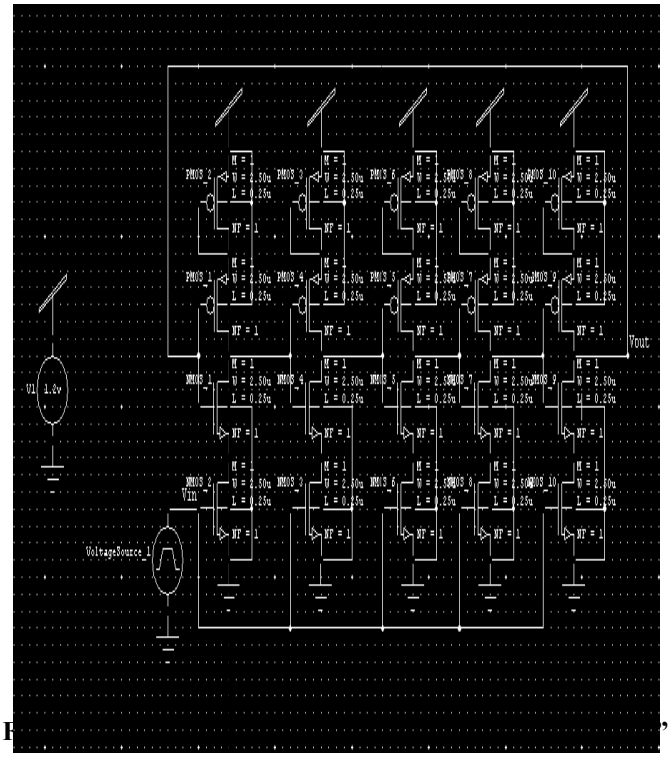
Figure 7: "Voltage vs. Frequency Plot of VCO with gates of PMOS transistors grounded"

5. VCO WITH PMOS TRANSISTORS DIODE CONNECTED

Figure 8 depicts the VCO with PMOS transistor diode connected. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria.

5.1 Simulation Results

Figure 9 shows the simulated waveform of proposed VCOperformed after the transient analysis of PMOS transistor diode connected with pulse input voltage, simulated using Tanner EDA ver. 13 simulator. In this VCO, gates of upper PMOS transistors are connected to their drains. The source voltage is applied to the gates of lower NMOS transistors.



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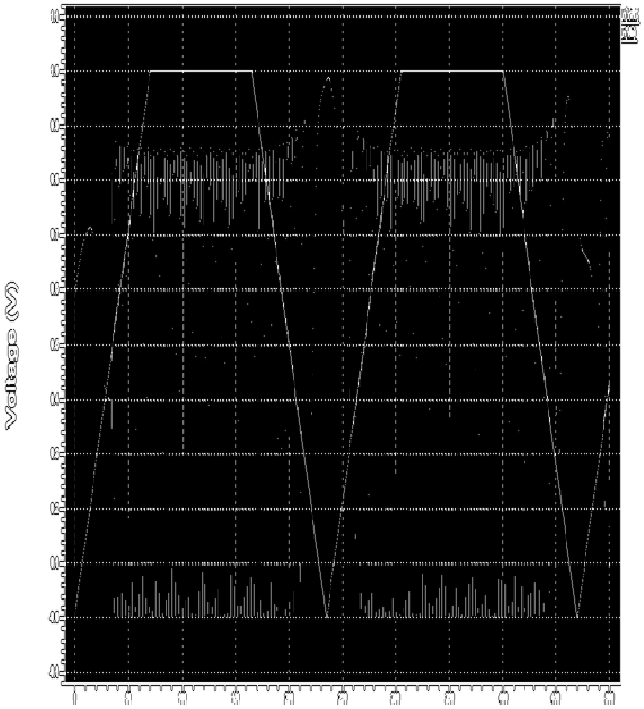

Figure 9: "Simulated results of proposed PMOS transistor diode connected VCO"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.15	38.4	0.026	0.00246
2.	0.2	27.7	0.036	0.0608
3.	0.3	7.87	0.12	0.4563
4.	0.4	5.58	0.179	1.21
5.	0.5	3.89	0.25	2.64
6.	0.6	3.49	0.28	4.25
7.	0.7	3.31	0.30	6.21
8.	0.8	3.16	0.31	8.38
9.	0.9	3.125	0.32	10.951
10.	1.0	3.07	0.32	13.52
11.	1.1	2.95	0.33	16.89
12.	1.2	2.94	0.34	20.68

Table 3: "Frequency & Dynamic Power Dissipation of VCO VCO with PMOS Transistor Diode Connected"

A graph is plotted between voltage and frequency, which is shown in the Figure 10, in order to observe the relation between these two quantities.

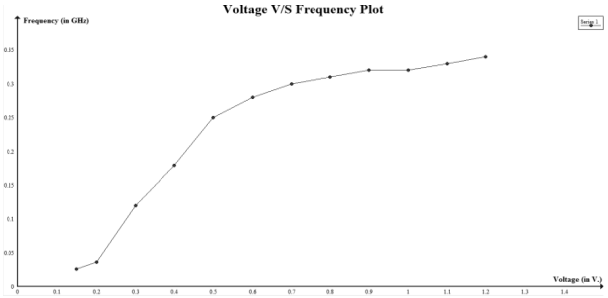

Figure 10: "Voltage vs. Frequency Plot of VCO with PMOS Transistor Diode Connected"

6. VCO WITH NMOS TRANSISTORS DIODE CONNECTED

Figure 11 depicts the VCO with NMOS transistor diode connected. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria. VCO circuit is simulated using Tanner EDA T-spice simulator ver 13.

6.1 Simulation Results

Figure 12 shows the simulated waveform of proposed VCOperformed after the transient analysis of NMOS transistor diode connected with pulse input voltage. In this VCO, gates of lower NMOS transistors are connected to their drains. The source voltage is applied to the gates of upper PMOS transistors.

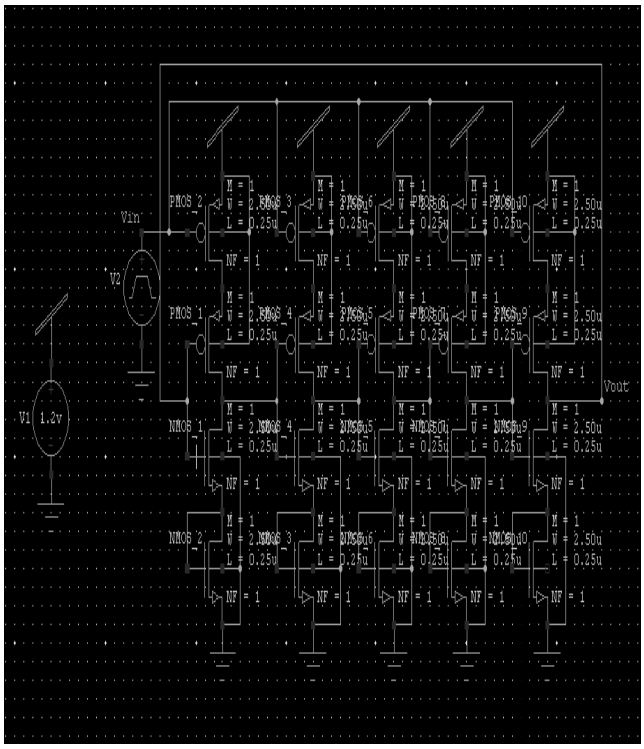

Figure 11: "Schematic Circuit of proposed VCO with NMOS transistors diode connected"

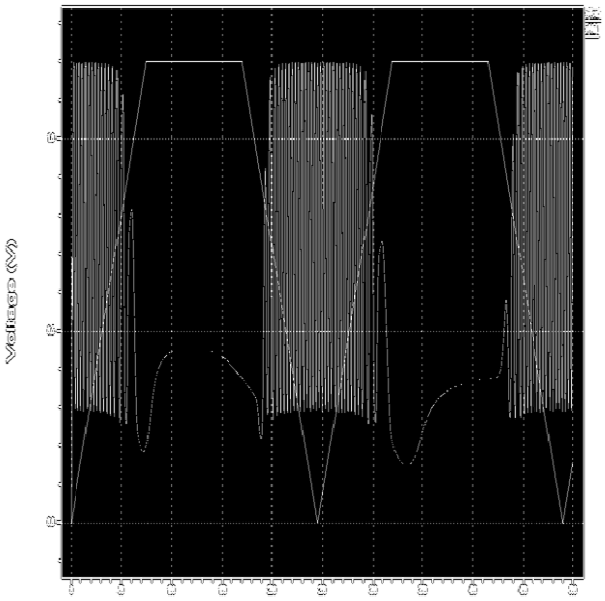

Figure 12: "Simulated results of proposed NMOS transistor diode connected VCO"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.12	3.10	0.322	0.019

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
2.	0.2	3.125	0.32	0.054
3.	0.3	3.14	0.31	0.11
4.	0.4	3.22	031	0.20
5.	0.5	3.33	0.30	0.31
6.	0.6	3.57	0.28	0.425
7.	0.7	4.18	0.23	4.7
8.	0.8	6.13	0.26	0.432
9.	0.9	9.25	0.10	0.34
10.	1.0	34.4	0.02	0.08
11.	1.1	-	0	0
12.	1.2	-	0	0

Table 4: "Frequency & Dynamic Power Dissipation of VCO VCO with NMOS Transistor Diode Connected"

A graph is plotted between voltage and frequency, which is shown in the Figure 13, in order to observe the relation between these two quantities.

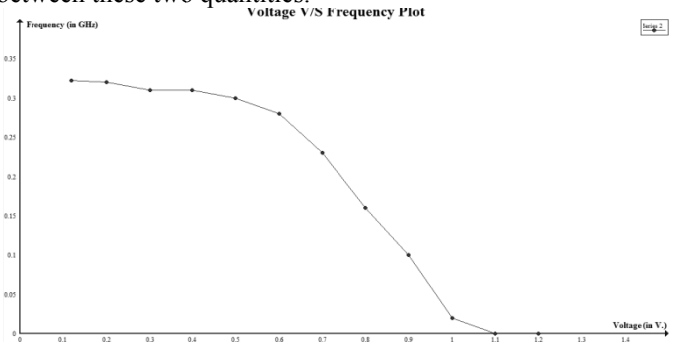

Figure 13: "Voltage vs. Frequency Plot of VCO with NMOS Transistor Diode Connected"

7. VCO WITH VOLTAGE APPLIED TO BOTH PMOS AND NMOS TRANSISTORS

Figure 14 depicts the VCO with voltage applied to both PMOS and NMOS transistors. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria. In this VCO, the two transistors M5 and M6 are eliminated and the source voltage is applied to the gates of both lower NMOS transistors and upper PMOS transistors.VCO circuit is simulated using Tanner EDA T-spice simulator ver 13.

7.1 Simulation Results

Figure 15 shows the simulated waveform of proposed VCO performed after the transient analysis of voltage applied to both PMOS and NMOS transistors with pulse input voltage. This VCO is having 380MHz of center frequency with 0.58uW.

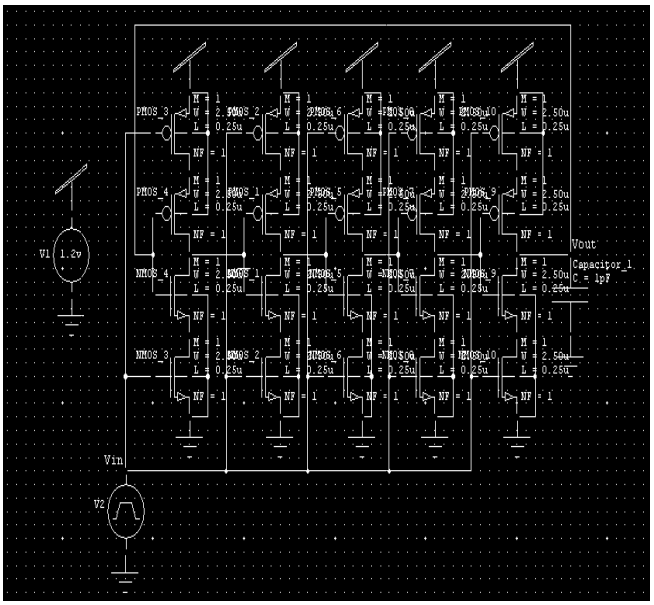

Figure 14: "Schematic Circuit of proposed VCO with voltage applied to both PMOS and NMOS transistors"

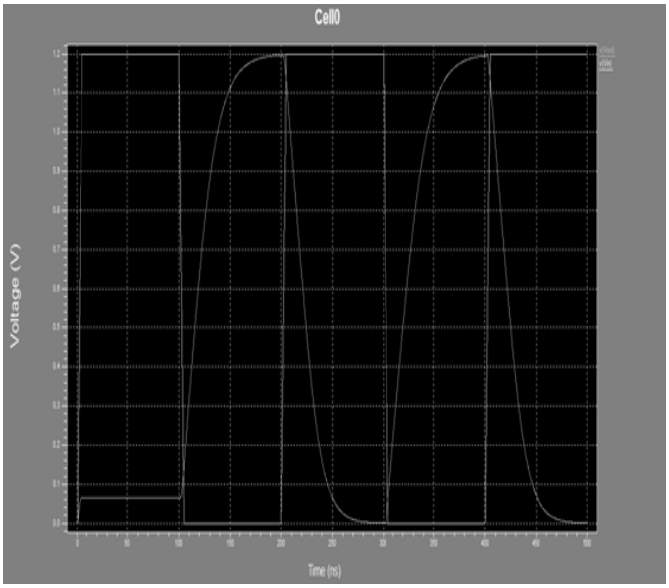

Figure 15: "Simulated results of proposed voltage applied to both PMOS and NMOS transistor VCO pulse input voltage"

A graph is plotted between voltage and frequency, which is shown in the Figure 16, in order to observe the relation between these two quantities.

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.1	1.96	0.51	0.0214
2.	0.2	2	0.5	0.084

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
3.	0.3	2.04	0.49	0.186
4.	0.4	2.22	0.45	0.304
5.	0.5	2.22	0.45	0.475
6.	0.6	2.77	0.36	0.547
7.	0.7	3.84	0.26	0.537
8.	0.8	5.88	0.17	0.456
9.	0.9	10.52	0.095	0.325
10.	1.0	40	0.025	0.105
11.	1.1	-	0	0
12.	1.2	-	0	0

Table 5: "Frequency & Dynamic Power Dissipation of voltage applied to both PMOS and NMOS transistor VCO"

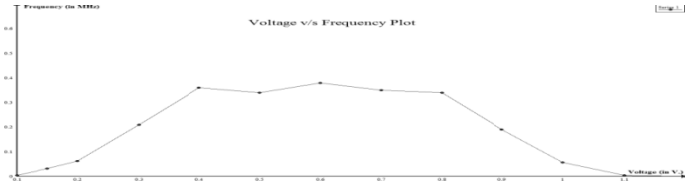

Figure 16: "Voltage vs. Frequency Plot of VCO with voltage applied to both PMOS and NMOS transistors"

8. COMPARATIVE ANALYSIS OF VOLTAGE VS FREQUENCY PLOTS OF RING OSCILLATOR VCO TOPOLOGIES

On the basis of results derived from graph plotted between the two critical parameters of ring oscillator VCO, dynamic power dissipation and frequency for different time and control voltages, for the various ring oscillator topologies, a table can is formed which compares the results of the topologies under consideration. Table 6 as shown below establishes the comparison.

S.No.	Topology	Frequency (in MHz)		Power Dissipation
		Fmin.	Fmax.	(uW)
1.	Current Starved VCO	0.011	0.54	0.57
2.	VCO with Gates of PMOS Transistor Grounded	0.01	0.57	0.60
3.	VCO with PMOS Diode Connected	0.026	0.34	4.25
4.	VCO with NMOS Diode Connected	0	0.32	4.25
5.	VCO with voltage applied to both PMOS and NMOS Transistor	0.005	0.38	0.58

Table 6: "Performance Comparison of topologies under consideration in terms of power and frequency"

The Table 6 results are plotted in the form of a graph, as shown in Figure 17, which establishes an excellent comparative study of Voltage Vs frequency plots of various ring topologies of VCO.

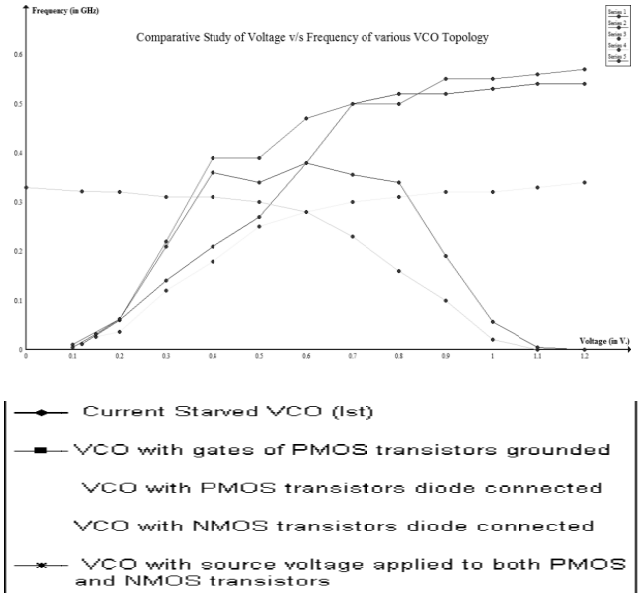

Figure 17: "Comparative analysis of Voltage Vs Frequency of various ring topology VCO"

9. CONCLUSION

The proposed work establishes the design and comparison of Current Starved VCO, VCO with Gates of PMOS Transistor Grounded, VCO with PMOS Diode Connected, VCO with NMOS Diode Connected, VCO with voltage applied to both PMOS and NMOS Transistor, totalling 5 different VCO topologies on the basis of their voltage, power and frequency in 70 nm CMOS technology. These VCO's topologies are designed using ring oscillator.

Different ring oscillator VCO topologies under consideration are simulated on Tanner EDA tool ver. 13. The supply voltage used for the simulation is 1.2 V. Different topologies exert different power dissipation and frequency characteristics. Their

performance comparison is obtained by plotting between voltage and dynamic power dissipation. Performance evaluation and comparison of different topologies results in minimum power consumption of 0.57 uW by Current Starved VCO topology and maximum operating frequency of 0.57 MHz by VCO with Gates of PMOS Transistor Grounded.

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