

Performance Comparison of XY, OE and DY Ad Routing Algorithm by Load Variation Analysis of 2-Dimensional Mesh Topology Based Network-on-Chip

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Submitted in August 2011; Accepted in January 2012

Abstract - Network on chip is a scalable and flexible communication architecture for the design of core based System-on-Chip. Communication performance of a NOC heavily depends on routing algorithm. XY routing algorithm is distributed deterministic routing algorithm. Odd-Even (OE) routing algorithm is distributed adaptive routing algorithm with deadlock-free ability. DyAD combines the advantages of both deterministic and adaptive routing schemes. Key metrics which determines best performance for routing algorithms for Network-on-Chip architectures are Minimum Latency, Minimum Power and Maximum Throughput. We demonstrated the impact of traffic load (bandwidth) variations on average latency and total network power for three routing algorithms XY, OE and DyAD on a 3x3 2-dimensional mesh topology. The simulation is performed on nirgam NoC simulator version 2.1 for constant bit rate traffic condition. The simulation results reveals the dominance of DyAD over XY and OE algorithms depicting the minimum values of overall average latency per channel (in clock cycles per flit) as 1.58871, overall average latency per channel (in clock cycles per packet) as 9.53226, overall average latency (in clock cycles per flit) as 26.105, and total network power as 0.1771 milliwatts, achieved for DyAD routing algorithm.

Index Terms - Network-on-chip; XY routing algorithm; OE routing algorithm; DyAD routing algorithm.

1. INTRODUCTION

Network on Chip (NoC) is a new paradigm for System on Chip (SoC) design [1-5]. With the growing complexity and increasing integration, the commonly used interconnection techniques for SoC architecture, bus structure, poses practical physical problems. In NoC paradigm, cores are connected to each other through a network of routers and they communicate among themselves through packet-switched communication. The protocols used in NoC are generally simplified versions of general communication protocols used in data networks. This makes it possible to use accepted and mature concepts of communication networks such as routing algorithms, switching techniques, flow and congestion control etc. in Network-on-

chip architecture. It allows significant reuse of resources and provides highly scalable and flexible communication infrastructure for SoC design.

Data communications between segments of chip are packetized and transferred through the network. The network consists of wires and routers. Processors, memories and other IP-blocks (Intellectual property) are connected to routers. A routing algorithm plays a significant role on network's operational performance.

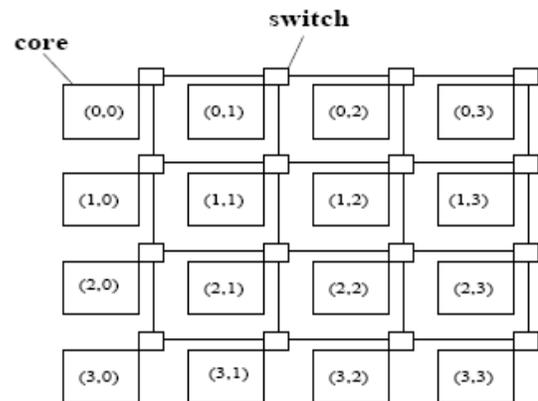


Figure 1: 4 X 4 2-Dimensional Mesh NoC

Different routing algorithms are targeted for different applications. Several routing algorithms need to be investigated and designed with various features and purposes.

The topic of Network on chip architecture is being introduced in this section. Section-2 explains about the three basic routing algorithms namely XY, Odd-even and DyAD routing algorithm in greater details. Section -3 describe architecture of a 3x3 2-dimensional mesh topology based NoC. Section -4 discusses simulation results and analysis of the proposed work. Section-5 ends with conclusion.

2. XY, OE AND DYAD ROUTING ALGORITHM

The routing algorithm, which defines the path taken by a packet between the source and the destination, is a main task in network layer design of NoC. According to where routing decisions are taken, it is possible to classify the routing as source and distributed routing [6].

Routing algorithm can be classified on the basis of adaptivity such as deterministic or adaptive. In deterministic routing, the path from source to destination is completely determined in advance by the source and destination address. Examples are XY routing. In adaptive routing, multiple paths from source to destinations are possible [7]. There also exists partially adaptive

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routing algorithms which restrict certain paths for communication with deadlock restrictions. Examples are Odd even routing. They are simple and easy to implement compared to adaptive routing algorithm. The routing algorithm that uses shortest path for communication is called minimal routing. The routing algorithm which uses longer paths for communication though shorter paths exist is known as non-minimal routing. Non-minimal routing has some advantages over minimal routing including possibility of balancing network load and fault tolerance. In static routing, the path cannot be changed after a packet leaves the source. In dynamic routing, a path can be altered anytime depending upon the network conditions. Routing algorithms can also be defined based on their implementation: lookup table and Finite State Machine (FSM). In the following text, three different routing algorithms are described in details:

2.1 XY Routing

The XY routing algorithm is one kind of distributed deterministic routing algorithm. XY routing never runs into deadlock or livelock [8]. For a 2-Dimension mesh topology NoC, each router can be identified by its coordinate (x, y) (Fig. 2). The XY routing algorithm compares the current router address (Cx,Cy) to the destination router address (Dx,Dy) of the packet, stored in the header flit [9]. Flits must be routed to the core port of the router when the (Cx,Cy) address of the current router is equal to the (Dx,Dy) address.

If this is not the case, the Dx address is firstly compared to the Cx (horizontal) address. Flits will be routed to the East port when $Cx < Dx$, to West when $Cx > Dx$ and if $Cx = Dx$ the header flit is already horizontally aligned. If this last condition is true, the Dy (vertical) address is compared to the Cy address. Flits will be routed to South when $Cy < Dy$, to North when $Cy > Dy$. If the chosen port is busy, the header flit as well as all subsequent flits of this packet will be blocked. The routing request for this packet will remain active until a connection is established in some future execution of the procedure in this router.

The following text is the XY routing algorithm:

```

/* XY routing Algorithm */
/*Source router: (Sx,Sy);destination router: (Dx,Dy); current
router: (Cx,Cy).*/
begin
if (Dx>Cx) //eastbound messages
return E;
else
if (Dx<Cx) //westbound messages
return W;
else
if (Dx=Cx) { //currently in the same column as
//destination
if (Dy<Cy) //southbound messages
return S;
else
if (Dy>Cy) //northbound messages
return N;

```

```

else
if (Dy=Cy) //current router is the destination router
return C;
}
end

```

The implementation of XY routing algorithm is simple. However, it is deterministic routing algorithm, which means this routing algorithm only provides a routing path for a pair of source and destination. Moreover, XY routing algorithm cannot avoid from deadlock appearance.

2.2 ODD-EVEN Routing (OE)

OE routing algorithm is a distributed adaptive routing algorithm which is based on odd-even turn model [10]. It exerts some restrictions, for avoiding and preventing from deadlock appearance. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels.

In a two-dimension mesh with dimensions $X*Y$ each node is identified by its coordinate (x, y) [9]. In this model, a column is called even if its x dimension element is even numerical column. Also, a column is called odd if its x dimension element is an odd number. A turn involves a 90-degree change of traveling direction. There are eight types of turns, according to the traveling directions of the associated channels. A turn is called an ES turn if it involves a change of direction from East to South. Similarly, we can define the other seven types of turns, namely EN, WS, WN, SE, SW, NE, and NW turns, where E, W, S, and N indicate East, West, South, and North, respectively. As a whole, there are two main theorems in odd-even algorithm:

Theorem1: No packet is permitted to do EN turn in each node which is located on an even column. Also, No packet is permitted to do NW turn in each node that is located on an odd column.

Theorem 2: No packet is permitted to do ES turn in each node that is in an even column. Also, no packet is permitted to do SW turn in each node which is in an odd column.

The following test is a minimal OE routing algorithm in which avail_dimension_set contains dimensions that are available for forwarding the packet:

```

/* OE routing algorithm */
/*Source router: (Sx,Sy);destination router: (Dx,Dy); current
router: (Cx,Cy).*/
begin
avail_dimension_set<-empty;
Ex<-Dx-Cx;
Ey<-Dy-Cy;
if (Ex=0 && Ey=0) //current router is destination
return C;
if (Ex=0){ //current router in same column as destination
if (Ey<0)
add S to avail_dimension_set;
else
add N to avail_dimension_set;

```

```

}
else{
if (Ex>0){ //eastbound messages
if (Ey=0){ //current in same row as destination
add E to avail_demision_set;
}
}
else{
if(Cx % 2 != 0 or Cx=Sx) //N/S turn allowed only in odd
column.
if(Ey < 0)
add S to avail_dimension_set;
else
add N to avail_dimension_set;
if(Dx% 2 != 0 or Ex != 1) {
//allow to go E only if destination is odd column
add E to avail_dimension_set;
//because N/S turn not allowed in even column
}
}
}
else { // westbound messages
add W to avail_dimension_set;
if(Cx%2=0) //allow to go N/S only in even column, because N-
>W and S->W
//not allowed in odd column
if(Ey<0)
add S to avail_dimension_set;
else
add N to avail_dimension_set;
}
}
//Select a dimension from avail_dimension_set to forward the
//packet.
End

```

OE routing algorithm is more complex than XY routing algorithm. However, it is one kind of adaptive routing algorithm. For a pair of source and destination, it can provide a group of routing paths and it can prevent from dead lock appearance.

2.3 DYAD Routing

DyAD combines the advantages of both deterministic and adaptive routing schemes [11]. DyAD is a routing technique which judiciously switches between deterministic and adaptive routing based on network congestion's conditions. Compared to purely adaptive routers, the overhead of implementing DyAD is negligible, while the performance is consistently better.

With DyAD routing each router in the network continuously monitors its local network load and makes decisions based on this information. When the network is not congested, a DyAD router works in a deterministic mode, thus enjoying the low routing latency enabled by deterministic routing. On the contrary, when the network becomes congested, the DyAD router switches back to the adaptive routing mode and thus

avoids the congested links by exploiting other routing paths; this leads to higher network throughput which is highly desirable for applications.

The freedom from deadlock and livelock [8] can be guaranteed when mixing deterministic and adaptive routing modes into the same NoC.

3. ARCHITECTURE OF 2 DIMENSION 3X3 MESH TOPOLOGY NOC

The routing Algorithm is simulated based on a 2-Dimension 3X3 mesh topology NoC (Fig. 2). In the Fig. 2, each circle represents a tile in the network. Each tile consists of an IP core connected to a router by a bidirectional core channel (C). A tile is connected to neighbor tiles by four bidirectional channels (N, E, S and W). Each tile is identified by a unique integer ID. Also, each tile can be identified by a pair x-coordinate and y-coordinate. Our 2-Dimesion 3X3 mesh topology NoC is designed using wormhole switching mechanism, in which packets are divided into flits. A packet consists of 3 types of flits, which are head flit, data flit and tail flit. All the three routing algorithms, XY routing algorithm, OE routing algorithm and DyAD routing algorithms are based on these characteristics.

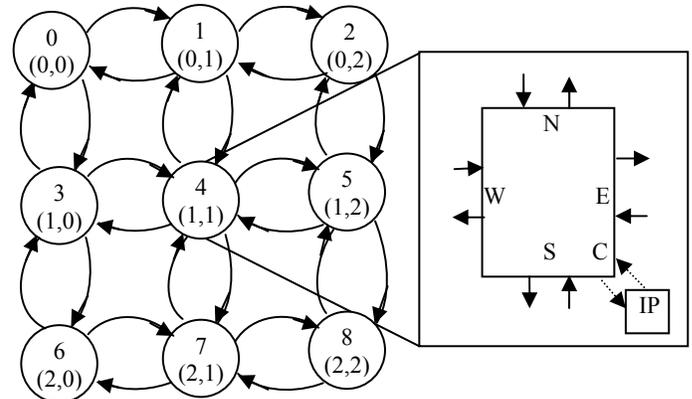


Figure 2: Architecture of a 2-dimensional 3x3 mesh topology based NoC

4. SIMULATION RESULTS AND ANALYSIS

The simulation is performed on NIRGAM simulator, a simulator for NoC Interconnect Routing and Application Modeling version 2.1. NIRGAM is an extensible and modular systemC based simulator [12] as has been depicted in Fig. 3. Simulations to all the three routing algorithms are performed under same traffic conditions and simulation control. Tiles are attached to constant bit rate (CBR) traffic generator. The packet size is of 20 bytes with random destination mode. The percentage load, maximum bandwidth to be utilized, is varied beginning with 10 % to 100 % in the steps of 10 %. The interval between two successive flits is 2 clock cycles. Simulation runs for 50000 clock cycles and the clock frequency is 1 GHz. Synthetic traffic generators generate traffic

in the first 3000 clock cycles with warm-up period of 800 clock cycles.

Fig. 3 shows the utilization of simulator for the proposed work elaborating the inputs given to the simulator and outputs taken from the simulator. There are two key measures of Performance of routing algorithms namely, overall average latency & total network power. The overall average latency in clock cycles per flit is also measured on a per channel basis on clock cycles per flit and clock cycles per packet. Total network power is measured in the units of milliWatts.

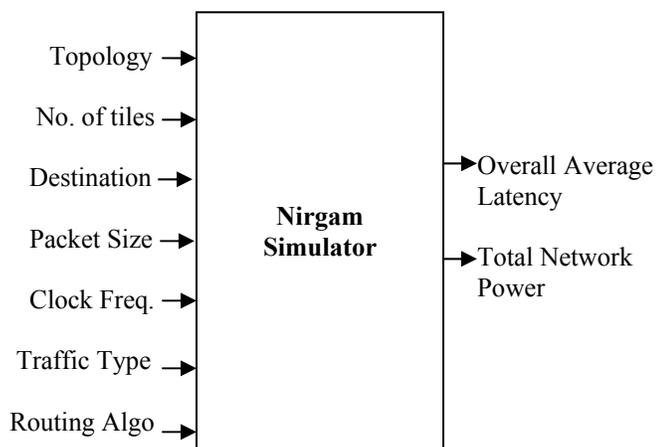


Figure3: Inputs and Outputs to Nirgam NoC Simulator

Table 1 depicts Simulation results for a 3x3 mesh topology NoC by comparing the impact of Load variation (bandwidth variation) on overall average latency per channel (in clock cycles per flit) for XY, OE and DyAd routing algorithms.

Fig.4. shows the graphical representation for simulation data of Table 1 shows Percentage Load variation vs Overall average latency per channel (in clock cycles per flit) for OE, XY and DyAD routing algorithm.

Table 2 depicts Simulation results for a 3x3 mesh topology NoC by comparing the impact of Percentage Load variation (bandwidth variation) on overall average latency per channel (in clock cycles per packet) for XY, OE and DyAd routing algorithms.

Fig.5. shows the graphical representation for simulation data of Table 2 shows Percentage Load variation vs Overall average latency per channel (in clock cycles per packet) for OE, XY and DyAD routing algorithm.

Table 3 depicts Simulation results for a 3x3 mesh topology NoC by comparing the impact of Percentage Load variation (bandwidth variation) on Overall average latency (in clock cycles per flit) for XY, OE and DyAd routing algorithms.

Fig.6 shows the graphical representation for simulation data of Table 2 shows Load vs Overall average latency (in clock cycles per flit) for OE, XY and DyAD routing algorithm.

Table 4 depicts Simulation results for a 3x3 mesh topology NoC by comparing the impact of Percentage Load variation

(bandwidth variation) on Total Network Power for XY, OE and DyAd routing algorithms.

Fig.7. shows the graphical representation for data of Table 4 shows Percentage Load variation vs Total Network Power for OE, XY and DyAD routing algorithm.

5. CONCLUSION

The routing algorithm is one of network layer researches of a NoC design, whose design approach can be adapted from a protocol stack including physical layer, data link layer, network layer and transport layer. Based on a 2-Dimension 3x3 mesh topology NoC, three different routing algorithms, XY routing algorithm, OE routing algorithm and DyAD routing algorithm are simulated on NIRGAM simulator platform and impact of Percentage Load variation is compared with four different parameters namely overall average latency per channel per packet, overall average latency per channel per flit, overall average latency per flit and overall network power respectively. The performance evaluation and the impact of Percentage Load variation (bandwidth variation) among the routing algorithms for two important parameters, overall average latency and overall network power are considered important design criteria to judge simulator as well as routing algorithm in the NoC research.

The minimum value of overall average latency per channel (in clock cycles per flit) is obtained as 1.58871, overall average latency per channel (in clock cycles per packet) is obtained as 9.53226, overall average latency (in clock cycles per flit) is obtained as 26.105, and total network power is obtained as 0.1771 milliwatts, achieved for DyAD routing algorithm. Thus proposed work shows the dominance of DyAD routing algorithm over OE and XY routing algorithms.

Thus it is concluded that compared to both deterministic and adaptive routing, significant performance improvements in terms of total network power as well as overall average latency can be achieved by using the DyAD approach for constant bit rate traffic conditions.

FUTURE SCOPE

Our conclusions are just fit for a 2-Dimension 3x3 mesh topology NoC. For other topologies, as well as taking into consideration other parameters, additional work needs to be done in the future.

REFERENCES

- [1]. P. Guerrier and A. Greiner, "A generic architecture for on-chip packet-switched interconnections," Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE 2000), Mar. 2000, pp. 250–256, doi:10.1109 / DATE. 2000.840047.
- [2]. A. Hemani, A. Jantsch, S. Kumar, A. Postula, J. Oberg, M. Millberg. et al, "Network on a chip: an architecture for billion transistor era," Proc. IEEE NorChip, 2000.

[3]. W. Dally and B. Towles, "Route packets, not wires: on-chip interconnection networks," Proc. Design Automation Conference, Jun.2001, pp. 684–689.

[4]. M. Sqroi, M. Sheets, A. Mihal, K. Keutzer, S. Malik, J.Rabaey, et al. "Addressing the system-on-a-chip interconnect woes through communication-based design",Proc. Design Automation Conference, Jun 2001, pp.667-672.

[5]. S. Kumar, A. Jantsch, J. Soinin, M. Forsell, M. Millberg, J. Oberg. et al, "A network on chip architecture and design methodology," Proc. IEEE Computer Society Annual Symposium on VLSI, Apr. 2002, pp. 105–112, doi: 0.1109/ISVLSI.2002.1016885.

[6]. J. Duato, S. Yalamanchili, L. Ni, Interconnection networks: an engineering approach, Morgan Kaufmann, Revised Edition, 2002.

[7]. L. M. Ni, P. K. Mckinley, "A Survey of Wormhole Routing Techniques in Direct Networks", Computer, vol. 26(2),Feb 1993, pp. 62 –76, doi: 10.1109/2.191995.

[8]. M. Dehyadgari, M. Nickray, A. Afzali-kusha, Z. Navabi:Evaluation of Pseudo Adaptive XY Routing Using an Object Oriented Model for NOC. The 17th International Conference on Microelectronics, 13–15December 2005.

[9]. Wang Zhang, Ligang Hou, Jinhui Wang, Shuqin Geng, Wuchen Wu, "Comparison Research between XY and Odd-Even Routing Algorithm of a 2-Dimension 3X3 Mesh Topology Network-on-Chip", WRI Global Congress on Intelligent Systems, GSIS'09, May 2009, pp. 329-333, doi: 10.1109/GCIS.2009.110.

[10]. Ge-Ming Chiu, "The odd-even turn model for adaptive routing", IEEE Transactions on parallel and distributed systems, Jul 2000, pp. 729-738 doi: 10.1109/71.877831.

[11]. Jingcao Hu; Marculescu, R., "DyAD - smart routing for networks-on-chip", 41st Proceeding of Design automation conference, San Diego, CA, USA, Jul 2004, pp. 260-263.

[12]. L. Jain., "NIRGAM: A Simulator for NoC Interconnect Routing and Applications Modeling", date conference, Sep 2007, pp. 1-2.

Load Variati on in %	Overall average latency per channel (in clock cycles per flit)		
	OE	XY	DyAD
10	1.89210	1.90542	1.58871
20	1.77547	2.01144	1.59463
30	1.90437	1.97100	1.59589
40	1.89210	2.02207	1.58785
50	2.07681	2.19148	1.58624
60	2.07850	2.17938	1.60494

Load Variati on in %	Overall average latency per channel (in clock cycles per flit)		
	OE	XY	DyAD
70	2.09805	2.09641	1.60256
80	2.13320	2.21263	1.61754
90	2.07522	2.23316	1.58733
100	2.61783	2.69170	1.94854

Table1: Simulation results for load variation verses overall average latency per channel (in clock cycles per flit) for XY, OE and DyAd routing algorithms

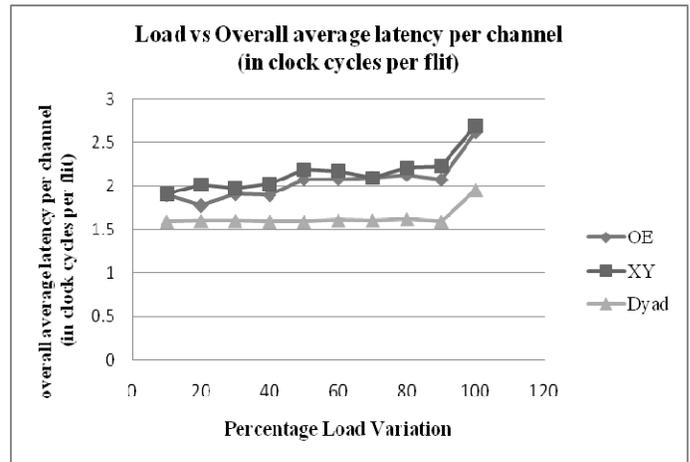


Figure4: Graph of Percentage Load variation vs Overall average latency per channel (in clock cycles per flit) for OE, XY and DyAD routing algorithm

Load Variati on in %	Overall average latency per channel (in clock cycles per packet)		
	OE	XY	DyAD
10	11.35260	11.43250	9.53226
20	10.65280	12.06860	9.56780
30	11.42620	11.82600	9.57534
40	11.35260	12.13240	9.52709
50	12.46080	13.14890	9.51746
60	12.47100	13.07630	9.62963
70	12.58830	12.57840	9.61539
80	12.79920	13.27580	9.70526
90	12.45130	13.39900	9.52396
100	15.70700	16.15020	11.69130

Table2: Simulation Data results for load variation verses overall average latency per channel (in clock cycles per packet) for XY, OE and DyAd routing algorithms.

Performance Comparison of XY, OE and DY Ad Routing Algorithm by Load Variation Analysis of 2-Dimensional Mesh Topology Based Network-on-Chip

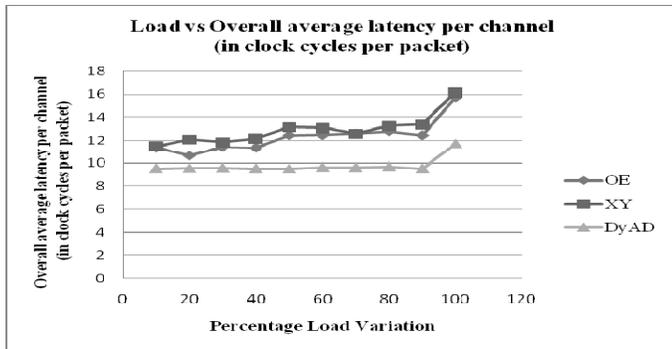


Figure5: Graph of Percentage Load variation vs Overall average latency per channel (in clock cycles per packet) for OE, XY and DyAD routing algorithm.

Load Variation in %	Overall average latency (in clock cycles per flit)		
	OE	XY	DyAD
10	30.49320	27.67840	26.10530
20	29.43840	29.04600	25.51350
30	30.77460	29.38890	25.39130
40	31.22220	29.73060	26.19350
50	34.74990	32.62700	27.58700
60	34.25790	32.04840	26.08700
70	34.40660	30.04250	26.25000
80	34.86770	31.81370	25.06520
90	34.46610	32.70150	27.40220
100	49.16410	44.60930	35.58830

Table3: Simulation results for Percentage Load variation versus Overall average latency (in clock cycles per flit) for XY, OE and DyAD routing algorithms

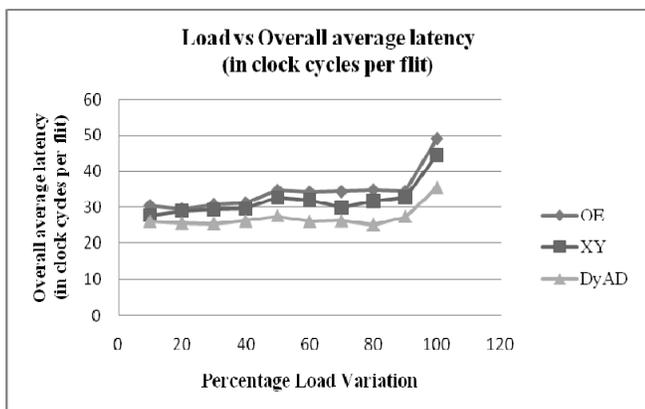


Figure6: Graph of Percentage Load variation vs Overall average latency (in clock cycles per flit) for OE, XY and DyAD routing algorithm.

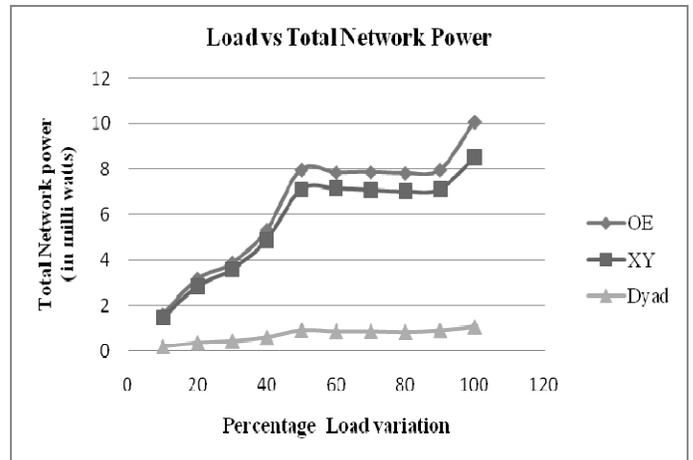


Figure7: Graph of Percentage Load variation vs Total Network power (in milliwatts) for OE, XY and DyAD routing algorithm

Load Variation in %	Total Network Power (milliwatts)		
	OE	XY	DyAD
10	1.58082	1.44145	0.17711
20	3.16042	2.83479	0.33712
30	3.85637	3.58444	0.41713
40	5.29437	4.86061	0.57989
50	7.96849	7.08161	0.89983
60	7.84587	7.13445	0.84869
70	7.86563	7.06261	0.85435
80	7.81336	7.00110	0.81458
90	7.96460	7.10278	0.89415
100	10.08040	8.54200	1.04783

Table4: Simulation results for Percentage Load variation versus Total Network power for XY, OE and DyAD routing algorithms