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CONTENTS

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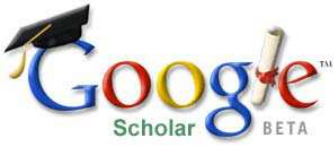

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Editorial

It is a matter of both honor and pleasure for us to put forth the eight issue of BIJIT; the BVICAM's International Journal of Information Technology. It presents a compilation of nine papers that span a broad variety of research topics in various emerging areas of Information Technology and Computer Science. Some application oriented papers, having novelty in application, have also been included in this issue, hoping that usage of these would further enrich the knowledge base and facilitate the overall economic growth. This issue shows our commitment in realizing our vision "to achieve a standard comparable to the best in the field and finally become a symbol of quality".

As a matter of policy of the Journal, all the manuscripts received and considered for the Journal by the editorial board are double blind peer reviewed independently by at-least two referees. Our panel of expert referees posses a sound academic background and have a rich publication record in various prestigious journals representing Universities, Research Laboratories and other institutions of repute, which, we intend to further augment from time to time. Finalizing the constitution of the panel of referees, for double blind peer review(s) of the considered manuscripts, was a painstaking process, but it helped us to ensure that the best of the considered manuscripts are showcased and that too after undergoing multiple cycles of review, as required.

The nine papers that were finally published were chosen out of seventy six papers that we received from all over the world for this issue. We understand that the confirmation of final acceptance, to the authors / contributors, sometime is delayed, but we also hope that you concur with us in the fact that quality review is a time taking process and is further delayed if the reviewers are senior researchers in their respective fields and hence, are hard pressed for time.

We further take pride in informing our authors, contributors, subscribers and reviewers that the journal has been indexed with some of the world's best international publishers like EBSCO (USA), Cabell's Directory (USA), DOAJ (Sweden), Google Scholar and J-Gate. It will certainly further increase the referencing of the papers published in this journal thereby enhancing the impact factor.

We wish to express our sincere gratitude to our panel of experts in steering the considered manuscripts through multiple cycles of review and bringing out the best from the contributing authors. We thank our esteemed authors for having shown confidence in BIJIT and considering it a platform to showcase and share their original research work. We would also wish to thank the authors whose papers were not published in this issue of the Journal, probably because of the minor shortcomings. However, we would like to encourage them to actively contribute for the forthcoming issues.

The undertaken Quality Assurance Process involved a series of well defined activities that, we hope, went a long way in ensuring the quality of the publication. Still, there is always a scope for improvement, and so, we request the contributors and readers to kindly mail us their criticism, suggestions and feedback at bijit@bvicam.ac.in and help us in further enhancing the quality of forthcoming issues.

Editors

CONTENTS

Performance Analysis of Variation in Power Consumption and Frequency on Different Topologies of Ring VCO in 70 nm CMOS Technology

Shitesh Tiwari[1], Parag Parandkar[2] and **Sumant Katiyal[3]**

Submitted in January 2012; Accepted in April 2012

Abstract - ***The proposed work describes the performance evaluation of different types of ring oscillator Voltage Controlled Oscillator topologies on the basis of two characteristic parameters power and frequency in 70 nm CMOS technology. The various topologies analyzed include Current Starved VCO, VCO with Gates of PMOS Transistor Grounded, VCO with PMOS Diode Connected, VCO with NMOS Diode Connected, VCO with voltage applied to both PMOS and NMOS Transistor. Simulation of different parameters of ring oscillator VCO is carried out on Tanner tool Version 13. VCO topologies are evaluated on the basis of frequency and power consumption by taking lower supply voltage of 1.2 V. Performance evaluation and comparison of different topologies results in minimum power consumption of 0.57 uW by Current Starved VCO topology and maximum operating frequency of 0.57 MHz by VCO with Gates of PMOS Transistor Grounded.***

Index Terms - Current Starved VCO, VCO With Gates of PMOS Transistors Grounded, VCO With PMOS Transistors Diode Connected,VCO With NMOS Transistors Diode Connected, VCO With Voltage Applied To Both PMOS And NMOS Transistors

1. INTRODUCTION

An oscillator that can be tuned over a wide range of frequencies by applying a voltage (tuning voltage) to it, or in other words, an oscillator that changes its frequency according to a control voltage feed to its control input is Voltage Controlled Oscillator [1]. As shown in Figure 1, the frequency of oscillation is varied by the applied controlled voltage, while modulating signals may also be fed into the VCO to cause frequency modulation (FM) or phase modulation (PM)[2][24]; a VCO with digital pulse output may similarly have its repetition rate (FSK, PSK) or pulse width modulation (PWM). The oscillator first convert voltage signal to current, and then current is converted into frequency [1]. This has numerous applications ranging from frequency synthesizers to transceivers. The design of high performance monolithic VCO has been one of the active area of research and development in recent years[22]. A CMOS VCO can be built using ring topology, relaxation circuits or LC tuned circuit [2]. The equation (1) shows the basic definition of VCO according to its operation forming a characteristic between input voltage and frequency.

$$W_{out} = W_o + K_{vco} * V_{control} \cdots\cdots\cdots \quad (1)$$

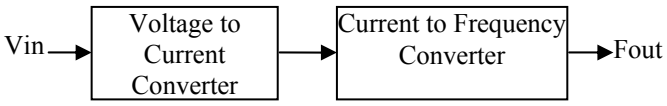

Figure 1: "Definition of VCO"

Here, W_o represents the intercept corresponding to $V_{control} = 0$ and K_{vco} denotes the 'gain' and 'sensitivity' of the circuit [2]. There are basically two types of Harmonic oscillators, LC and Ring Oscillator. The main advantage of Ring oscillator over LC oscillator is that the ring oscillator can be easily fabricated in CMOS technology as compared to LC oscillator, since the fabrication of inductor need huge amount of space [5][24].

2. DEVELOPMENT OF NEW DESIGN METHODOLOGY FOR OPTIMIZATION OF POWER WITH LOW VOLTAGE

The general source of dissipation in any CMOS circuit is the current drawn while switching. Since knowing the number and capacitance, the voltage change on a gate capacitance requires charge transfer and hence causes power consumption. Once this gate capacitance is charged, the gate can maintain the DC voltage level without any additional charge movement and does not consume any current. The required charge to change voltage levels on the gate is described by the following equation [18][24].

$$Qgate = Cgate\ V_{dd} \quad (2)$$

Qgate is the charge required to change state, Cgate is the gate capacitance, V_{dd} is the power supply voltage. Switching generates a current proportional to operating frequency (F) of the VCO. Since current is defined in terms of coulombs per second (amperes), the current can be calculated as shown in equation (4) [19].

$$I = Qgate \times Frequency = (Cgate \times V_{dd}) \times F \quad (3)$$

Where I is the current in amperes (coulombs per second)
The total current can be generalized into a figure which will include all the node capacitances in the device.

$$Idevice = Ctotal \times V_{dd} \times Fosc \quad (4)$$

where

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Idevice is the total device current,
Ctotal is the total node capacitance of all internal switching nodes,
Fosc is the switching frequency of the circuit.
All of the internal switching nodes are an unmanageable task; the current under different conditions can be determined empirically by measuring the current level for a particular known frequency and supply voltage conditions, and then scaling the current value to determine the behavior under different conditions [23]. The dependency of these currents is directly on the system operation and the supply levels [25].
The VCO power dissipation is function of its frequency hence should be modeled with care.
Average Power Dissipation = $Fosc.N.C.V_{dd}$ (5)
Here Fosc is the oscillaton frequency, C is the device capacitance and N may be the number of stages in case of a ring oscillator.
Assuming the inverters are identical, the oscillation frequency is given in equation below,

$$f_{osc} = 1/(n^* (t_{phl} + t_{plh})) \quad (6)$$

Where n is the number of inverters in the ring oscillator and $(t_{phl} + t_{plh})$ is the propagationdelay time of each inverter. The propagation delay times t_{phl} and t_{plh} determine the input to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively
Ring oscillator is designed by using five CMOS inverters having

$$(W/L)p=12/2 \text{ and } (W/L)n=5/2. \quad (7)$$

These specifications are chosen in the relation

$$(W/L)p=2.5\ (W/L)n \quad (8)$$

by applying condition for symmetric inverter i.e. $K_n=K_p$. By taking these values of W/L, if the DC characteristics of CMOS inverter are observed switching point is found to closer to $2.5(V_{dd}/2=5/2)$.
The performance evaluation and comparison on the basis of two critical parameters, power consumption and frequency, of following topologies of ring type VCOs are discussed in the proposed work [24].

- Current Starved VCO
- VCO with gates of PMOS transistors grounded
- VCO with PMOS transistors diode connected
- VCO with source voltage applied to both PMOS and NMOS transistors
- VCO with NMOS transistors diode connected

In the further sections, proposed circuit schematic of the particular topology of ring oscillator, the associated simulation results and then the tabular representation of the input parameters control voltage and time, over which the parameters under consideration, power dissipation and frequency are calculated, and the respective voltage verses frequency graphs are drawn, which are discussed individually at length.

3. CURRENT STARVED VCO

Figure 2 depicts the proposed current starved VCO. It consists of five stage ring oscillator with a current mirror circuit. This ring oscillator is designed by taking into consideration odd number of inverters which form a closed loop with positive feedback. Transistor M5 and M6 form a current mirror circuit. PMOS transistor M3 and NMOS transistor M2 form an inverter while transistors M1 and M4 are used for biasing.

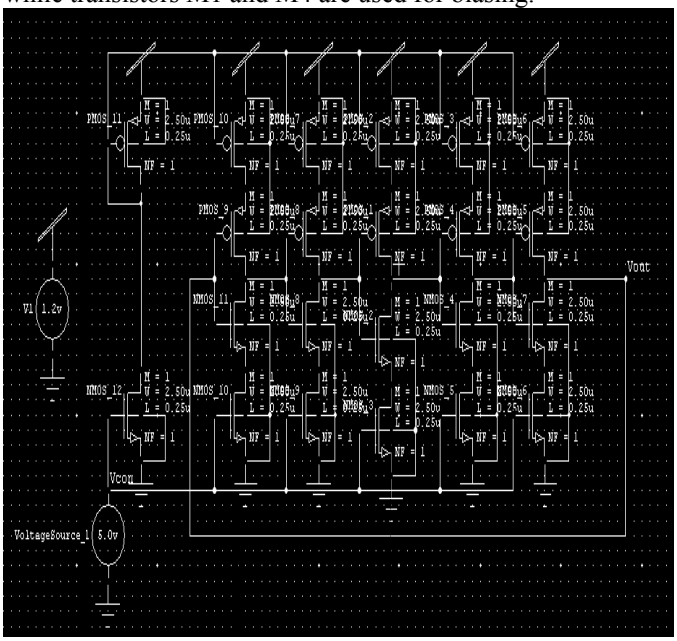


Figure 2: "Schematic circuit of Current Starved VCO"

3.1 Simulation Results:

Equation (1) defines the VCO in terms of control voltage and output frequency. This definition can be further developed for specific types of VCOs. For example equation (9) gives the output frequency of a current starved based stage selectable VCO [21].

$$f_{osc} = \beta\{ [(V_{con} - V_{ss}) - V_t][V_{DD} - V_{ss} - V_{gsp}]\}/N. C_{tot}. V_{DD} \text{ [9]}$$

Where f_{osc} is the output frequency generated by the VCO, β is the transconductance parameter, Vcon is the control voltage VDD & VSS are the power supplies, N is the number of stages, Ctot is the total capacitance on drains of MOSFETs and V_{gsp} is gate to source voltage of PMOS.
The current starved VCO circuit, performed after the transient analysis of current starved VCO with pulse input voltage, simulated using Tanner EDA ver. 13 T-spice simulator as shown in the figure 2. The number of stages of ring oscillator was optimized with center frequency of 380 Mhz. The current starved VCO draws 100uA drain current from supply voltage of 1.2V.

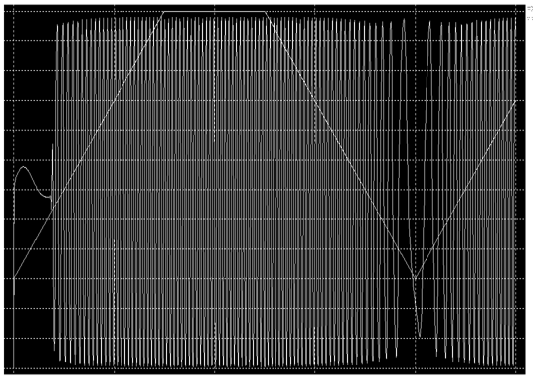


Figure 3: "Simulation results of proposed current starved VCO"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.1	500	.011	0.0006
2.	0.2	16.66	0.06	0.01
3.	0.3	7.1	0.14	0.053
4.	0.4	4.8	0.21	0.14
5.	0.5	3.70	0.27	0.28
6.	0.6	2.63	0.38	0.57
7.	0.7	2.0	0.5	1.3
8.	0.8	1.92	0.52	1.4
9.	0.9	1.92	0.52	1.5
10.	1.0	1.88	0.53	2.23
11.	1.1	1.85	0.54	2.76
12.	1.2	1.85	0.54	3.2

Table 1: "Frequency & Dynamic Power Dissipation of Current Starved VCO"

A graph is plotted between voltage and frequency as shown in the Figure 4, in order to observe the relation between these two quantities.

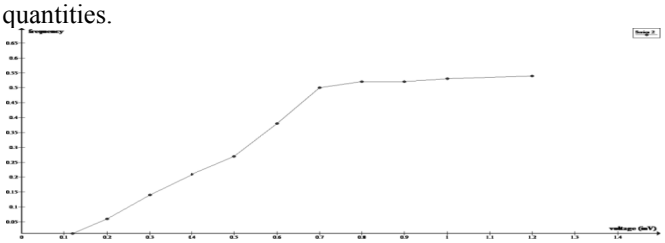


Figure 4: "Voltage vs. Frequency Plot of Current Starved VCO"

4. VCO WITH GATES OF PMOS TRANSISTORS GROUNDED

Figure 5 depicts the proposed VCO with gates of PMOS transistors grounded. It consists of five stage ring oscillator. This ring oscillator made by odd number of inverters which forms a closed loop with positive feedback.In this type of VCO, PMOS transistor is always ON since the gate terminal of PMOS transistor is connected to ground and PMOS transistor gives strong 1, so it behaves as a resistor.

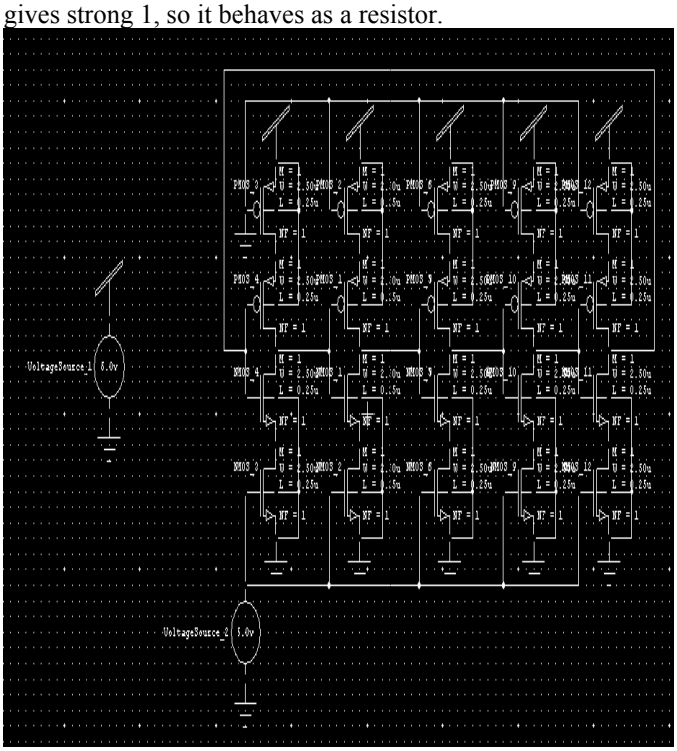


Figure 5: "Schematic Circuit of proposed VCO with gates of PMOS Transistors Grounded"

4.1 Simulation Results

The VCO with gates if PMOS transistors grounded performed after the transient analysis of PMOS transistor grounded with pulse input voltage, simulated using Tanner EDA ver. 13 simulator is as shown in the following Figure 5. The number of stages of ring oscillator was optimized with a center frequency of 470MHz. The VCO with gates of PMOS transistors grounded draws 100uA of drain current from a supply voltage of 1.2V.

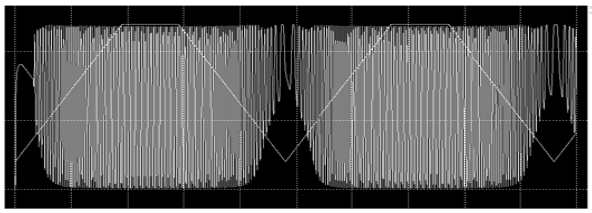


Figure 6: "Simulated results of proposed VCO with Gates of PMOS Transistor Grounded"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic Power Dissipation (uW)
1	0.1	100	0.01	0.0004
2	0.2	16.12	0.062	0.01
3	0.3	4.54	0.22	0.08
4	0.4	2.56	0.39	0.26
5	0.5	2.55	0.392	0.41
6	0.6	2.12	0.47	0.6
7	0.7	2.0	0.5	1.03
8	0.8	2.0	0.5	1.35
9	0.9	1.87	0.55	1.88
10	1.0	1.87	0.55	2.22
11	1.1	1.78	0.56	2.86
12	1.2	1.75	0.57	3.46

Table 2: "Frequency & Dynamic Power Dissipation of VCO with Gates of PMOS Transistor Grounded"

A graph is plotted between voltage and frequency, which is shown in the Figure 7, in order to observe the relation between these two quantities.

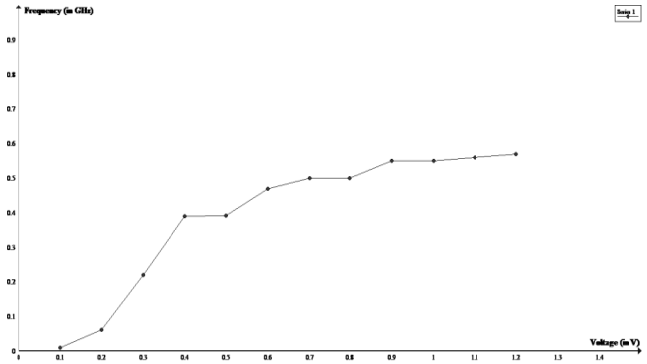


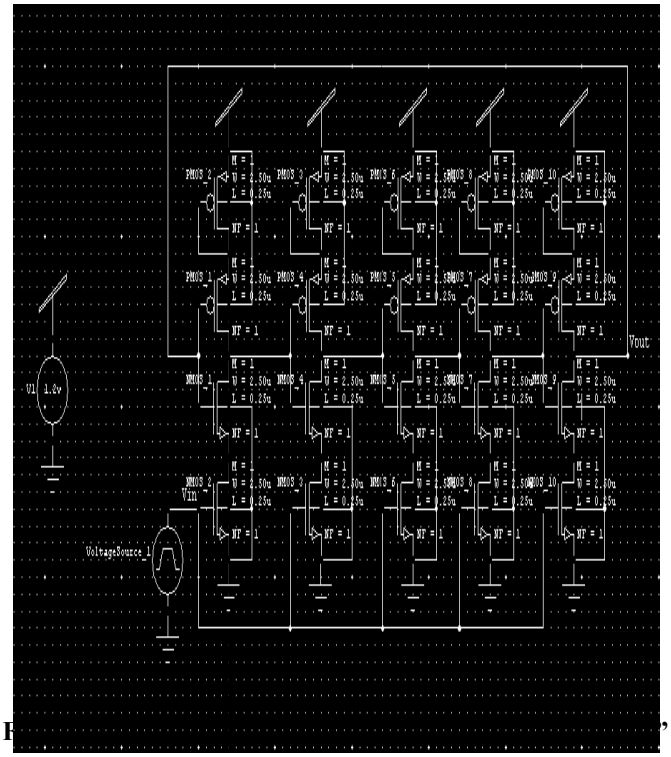
Figure 7: "Voltage vs. Frequency Plot of VCO with gates of PMOS transistors grounded"

5. VCO WITH PMOS TRANSISTORS DIODE CONNECTED

Figure 8 depicts the VCO with PMOS transistor diode connected. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria.

5.1 Simulation Results

Figure 9 shows the simulated waveform of proposed VCOperformed after the transient analysis of PMOS transistor diode connected with pulse input voltage, simulated using Tanner EDA ver. 13 simulator. In this VCO, gates of upper PMOS transistors are connected to their drains. The source voltage is applied to the gates of lower NMOS transistors.



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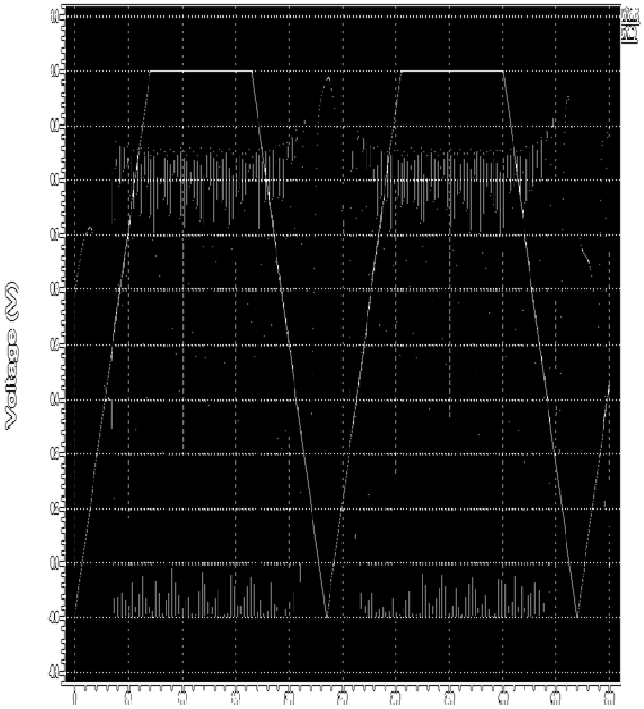

Figure 9: "Simulated results of proposed PMOS transistor diode connected VCO"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.15	38.4	0.026	0.00246
2.	0.2	27.7	0.036	0.0608
3.	0.3	7.87	0.12	0.4563
4.	0.4	5.58	0.179	1.21
5.	0.5	3.89	0.25	2.64
6.	0.6	3.49	0.28	4.25
7.	0.7	3.31	0.30	6.21
8.	0.8	3.16	0.31	8.38
9.	0.9	3.125	0.32	10.951
10.	1.0	3.07	0.32	13.52
11.	1.1	2.95	0.33	16.89
12.	1.2	2.94	0.34	20.68

Table 3: "Frequency & Dynamic Power Dissipation of VCO VCO with PMOS Transistor Diode Connected"

A graph is plotted between voltage and frequency, which is shown in the Figure 10, in order to observe the relation between these two quantities.

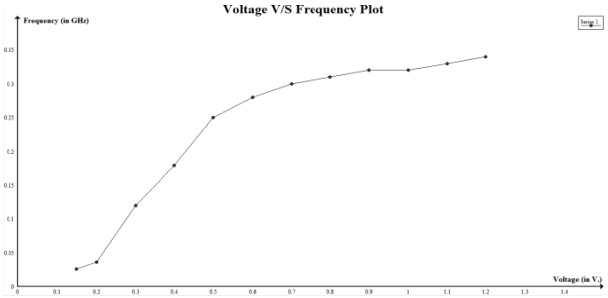

Figure 10: "Voltage vs. Frequency Plot of VCO with PMOS Transistor Diode Connected"

6. VCO WITH NMOS TRANSISTORS DIODE CONNECTED

Figure 11 depicts the VCO with NMOS transistor diode connected. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria. VCO circuit is simulated using Tanner EDA T-spice simulator ver 13.

6.1 Simulation Results

Figure 12 shows the simulated waveform of proposed VCOperformed after the transient analysis of NMOS transistor diode connected with pulse input voltage. In this VCO, gates of lower NMOS transistors are connected to their drains. The source voltage is applied to the gates of upper PMOS transistors.

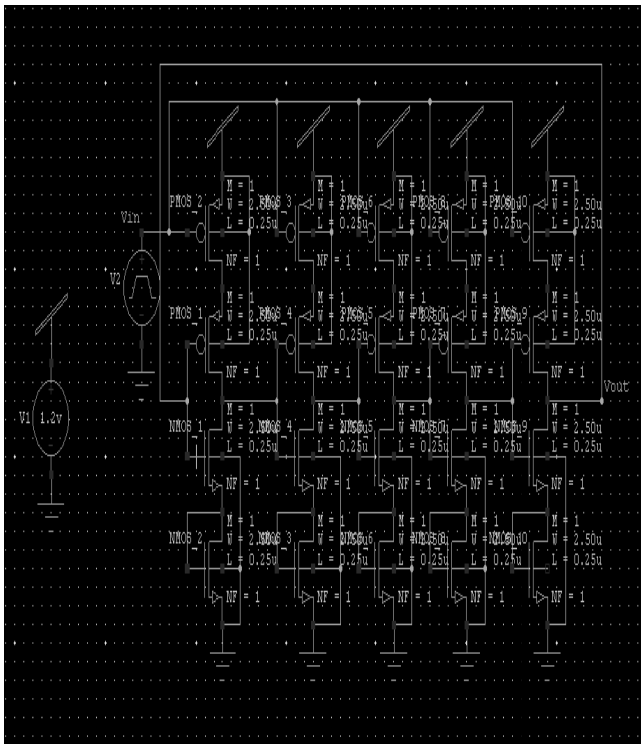

Figure 11: "Schematic Circuit of proposed VCO with NMOS transistors diode connected"

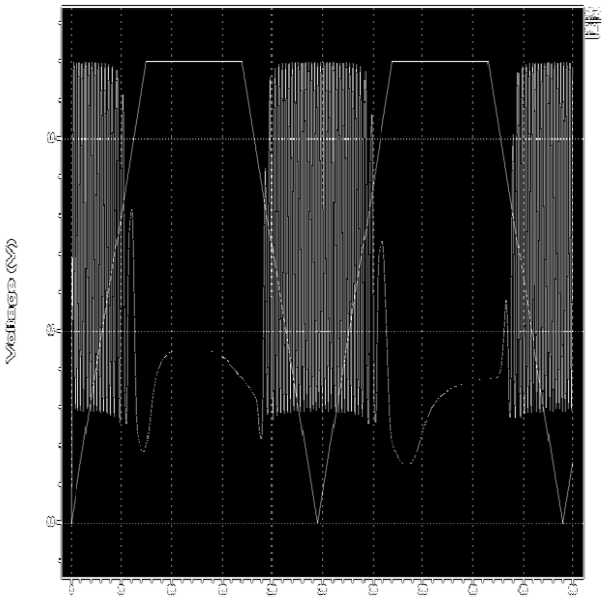

Figure 12: "Simulated results of proposed NMOS transistor diode connected VCO"

The summary of simulated result waveform is shown in table below:

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.12	3.10	0.322	0.019

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
2.	0.2	3.125	0.32	0.054
3.	0.3	3.14	0.31	0.11
4.	0.4	3.22	031	0.20
5.	0.5	3.33	0.30	0.31
6.	0.6	3.57	0.28	0.425
7.	0.7	4.18	0.23	4.7
8.	0.8	6.13	0.26	0.432
9.	0.9	9.25	0.10	0.34
10.	1.0	34.4	0.02	0.08
11.	1.1	-	0	0
12.	1.2	-	0	0

Table 4: "Frequency & Dynamic Power Dissipation of VCO VCO with NMOS Transistor Diode Connected"

A graph is plotted between voltage and frequency, which is shown in the Figure 13, in order to observe the relation between these two quantities.

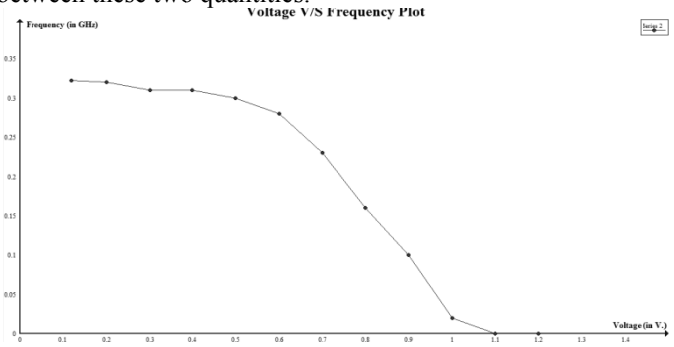

Figure 13: "Voltage vs. Frequency Plot of VCO with NMOS Transistor Diode Connected"

7. VCO WITH VOLTAGE APPLIED TO BOTH PMOS AND NMOS TRANSISTORS

Figure 14 depicts the VCO with voltage applied to both PMOS and NMOS transistors. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria. In this VCO, the two transistors M5 and M6 are eliminated and the source voltage is applied to the gates of both lower NMOS transistors and upper PMOS transistors.VCO circuit is simulated using Tanner EDA T-spice simulator ver 13.

7.1 Simulation Results

Figure 15 shows the simulated waveform of proposed VCO performed after the transient analysis of voltage applied to both PMOS and NMOS transistors with pulse input voltage. This VCO is having 380MHz of center frequency with 0.58uW.

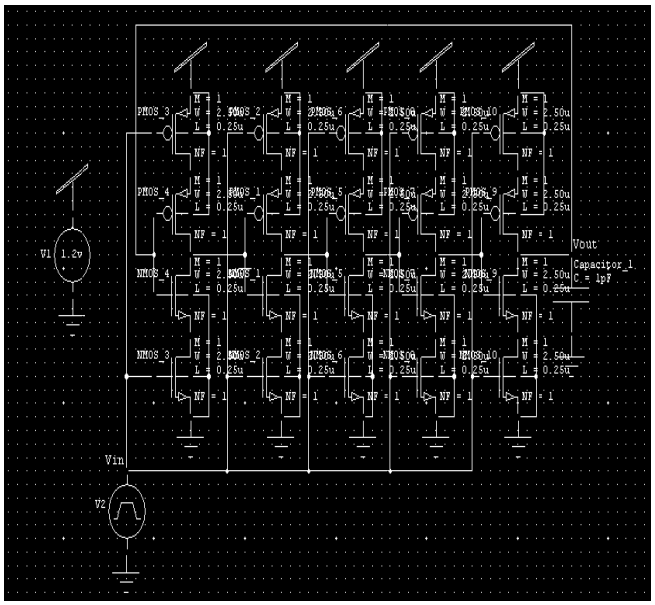

Figure 14: "Schematic Circuit of proposed VCO with voltage applied to both PMOS and NMOS transistors"

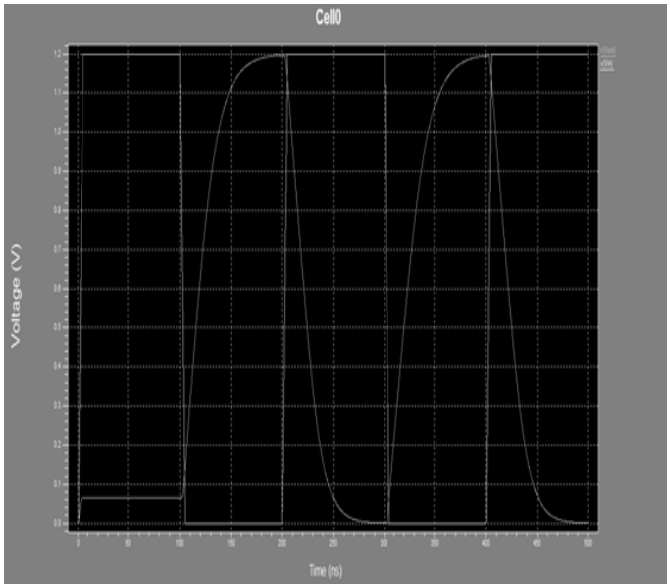

Figure 15: "Simulated results of proposed voltage applied to both PMOS and NMOS transistor VCO pulse input voltage"

A graph is plotted between voltage and frequency, which is shown in the Figure 16, in order to observe the relation between these two quantities.

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
1.	0.1	1.96	0.51	0.0214
2.	0.2	2	0.5	0.084

S.No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Dynamic power dissipation (uW)
3.	0.3	2.04	0.49	0.186
4.	0.4	2.22	0.45	0.304
5.	0.5	2.22	0.45	0.475
6.	0.6	2.77	0.36	0.547
7.	0.7	3.84	0.26	0.537
8.	0.8	5.88	0.17	0.456
9.	0.9	10.52	0.095	0.325
10.	1.0	40	0.025	0.105
11.	1.1	-	0	0
12.	1.2	-	0	0

Table 5: "Frequency & Dynamic Power Dissipation of voltage applied to both PMOS and NMOS transistor VCO"

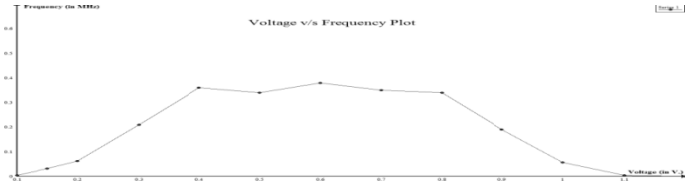

Figure 16: "Voltage vs. Frequency Plot of VCO with voltage applied to both PMOS and NMOS transistors"

8. COMPARATIVE ANALYSIS OF VOLTAGE VS FREQUENCY PLOTS OF RING OSCILLATOR VCO TOPOLOGIES

On the basis of results derived from graph plotted between the two critical parameters of ring oscillator VCO, dynamic power dissipation and frequency for different time and control voltages, for the various ring oscillator topologies, a table can is formed which compares the results of the topologies under consideration. Table 6 as shown below establishes the comparison.

S.No.	Topology	Frequency (in MHz)		Power Dissipation
		Fmin.	Fmax.	(uW)
1.	Current Starved VCO	0.011	0.54	0.57
2.	VCO with Gates of PMOS Transistor Grounded	0.01	0.57	0.60
3.	VCO with PMOS Diode Connected	0.026	0.34	4.25
4.	VCO with NMOS Diode Connected	0	0.32	4.25
5.	VCO with voltage applied to both PMOS and NMOS Transistor	0.005	0.38	0.58

Table 6: "Performance Comparison of topologies under consideration in terms of power and frequency"

The Table 6 results are plotted in the form of a graph, as shown in Figure 17, which establishes an excellent comparative study of Voltage Vs frequency plots of various ring topologies of VCO.

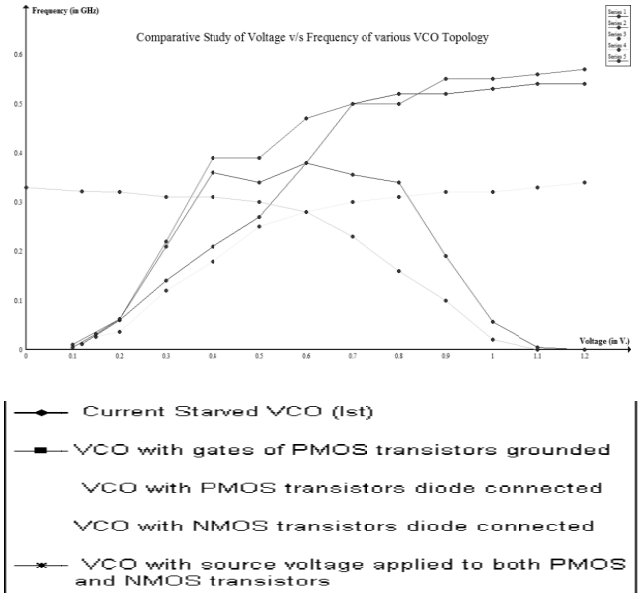

Figure 17: "Comparative analysis of Voltage Vs Frequency of various ring topology VCO"

9. CONCLUSION

The proposed work establishes the design and comparison of Current Starved VCO, VCO with Gates of PMOS Transistor Grounded, VCO with PMOS Diode Connected, VCO with NMOS Diode Connected, VCO with voltage applied to both PMOS and NMOS Transistor, totalling 5 different VCO topologies on the basis of their voltage, power and frequency in 70 nm CMOS technology. These VCO's topologies are designed using ring oscillator.

Different ring oscillator VCO topologies under consideration are simulated on Tanner EDA tool ver. 13. The supply voltage used for the simulation is 1.2 V. Different topologies exert different power dissipation and frequency characteristics. Their

performance comparison is obtained by plotting between voltage and dynamic power dissipation. Performance evaluation and comparison of different topologies results in minimum power consumption of 0.57 uW by Current Starved VCO topology and maximum operating frequency of 0.57 MHz by VCO with Gates of PMOS Transistor Grounded.

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Tracking Digital Footprints of Scareware to Thwart Cyber Hypnotism through Cyber Vigilantism in Cyberspace

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Abstract - The characteristics of the Internet, which include digitization, anonymity, connectivity, mobility, and transnational nature; blur the traditional model of crime investigation / law enforcement and call for new strategies. Many simple yet popular malicious activities over internet are carried out by scammers / con artists largely through electronic mails and websites using cyber hypnotism, often in combination with distribution and propagation of malware. Such crimes of persuasion need to be managed through due diligence. Recently, an added web-based threat is recognized in the form of scareware which is making even the savviest of computer users their victim, and therefore, there is a need to focus on trying to detect such suspicious activity as quickly as possible in order to shut it down. An in-depth analysis of few scareware reveal that they have created many new and not so widely recognized online threats with inside intelligence by providing primary delivery mechanism for malware such as rogue anti-virus and anti-spyware, which are beyond the reach of many legitimate anti-virus programs currently in use. They may cause a Denial of Service (DoS) attack forcing the system to crash or even a Distributed Denial of Service (DDoS) attack. Looking at such unprecedented challenges in cyberspace, a policy of cyber vigilantism adopting an active defense rather than a reactive approach is contemplated. It is felt that in this age of mobile workforce, many of such people working as cyber analytics, or cyber-crime researcher may accomplish this work of community policing and play as proactive guardians of cyberspace.

Index Terms - Internet, Cyber Hypnotism, Con Artist, Scareware, Cyber Vigilantism.

1. INTRODUCTION

The Internet, as understood today, is a vast global network of computers storing information on every conceivable subject of interest to humankind. Its' original designers aimed to create a communication system between trusted people and organizations for academic and military purposes resilient in the face of a nuclear attack. There were no views to the security of the computers attached to neither these networks nor the information stored in these computers. The commercial use of internet came as an afterthought. Today, it has evolved from a mere means of communication to an open and insecure system of worldwide network. Real world's constraints such as time and space do not exist on it. National boundaries have little meaning in cyberspace and information flows continuously and seamlessly across political, ethical and religious divides. Even the infrastructure that makes of cyberspace (software and hardware) is global in nature. Because of this global nature of cyberspace, the existing vulnerabilities are also open to the world and to anyone, anywhere, who has sufficient capability to exploit them. These infrastructures are, therefore, being continuously probed for weakness and vulnerability by new breed of professional cyber criminals primarily motivated by huge financial gains. In recent years, several electronic mail frauds and scareware, herein discussed as crimes of persuasion, have brought to light the darker side of the Internet.

This paper examines the concept that industry, government and the public are essentially naked in cyberspace, with privacy diminishing, identity theft increasing, financial accounts and intellectual property becoming highly vulnerable to cyber criminals. Taking lessons from real-world incidences, this paper discusses attackers' technique in general terms, more particularly related to cyber hypnotism (i.e., hypnotizing people through internet by exploiting various human weaknesses and emotional vulnerabilities in cyberspace) and related crimes of persuasion including email fraud besides scareware (a type of malware). In this context, Hypnotism, as understood, is "a wakeful state of focused attention and heightened suggestibility, with diminished peripheral awareness, usually induced by a procedure known as hypnotic induction, which is commonly composed of a long series of preliminary instructions and suggestions". This is in contrary to a popular misconception that hypnosis is a form of unconsciousness resembling sleep[1]. Malware, also known as malicious code & software (e.g., viruses, Trojan horse, worms, keyloggers, scareware, spyware etc.), meant specifically to damage or disrupt a system irreparably and to steal the personal information and address books existing on the system in cache memory / records, by hijacking the browser and redirect to a phishing – con webpage. Evidently, many cyber-crimes, largely carried out through a series of hypnotizing emails, are often associated with malwares and warrant a constant vigilance at individual level besides better technical controls. It is noteworthy that majority of such cyber-crimes do not require a high level of

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technical specification and can be prevented through 'due diligence', nevertheless, sophisticated cyber-crimes demand an altogether different approach. Cyber Vigilantism, as visualized in this communication, is " a proactive policy to attack the attackers in an ethical way with restraint in a limited manner rather than adopting a soft policy of passive reaction." In turn, it will encourage good guys into action and discourage the bad guys in the near future.

2. E-MAIL FRAUD AND CYBER HYPNOTISM

Cyber-crime is regarded as computer-mediated activities which are either illegal or considered illicit by parties and which can be conducted through global electronic networks[2]. Conceptually cyber-crimes differ little from traditional crimes as they frequently involve perpetrators who have no physical presence at or even near the crime scene. In such crimes when no direct physical evidence exists, inferential evidence, or evidence that some aspect of the system has been modified as a direct result of the intrusion, is the primary source of clues. In fact, cyber-attacks come in two forms: one against data, the other on control systems. The first type attempts to steal or corrupt data and deny services. The vast majority of internet and other computer attacks fall into this category. Individuals, who wish to use computer as a tool to facilitate unlawful activity are finding that the Internet provides a vast, inexpensive, and potentially anonymous way to commit unlawful acts. The Net enables transaction between people who do not know, and in many cases cannot know each other's physical location. As of 2012, the estimated number of Internet users worldwide reaches 2,267,233,742[3]. Most of these users have electronic mail (email) accounts on one or more mail systems and emails are being utilized by cyber criminals as the vehicle of persuasion. According to Symantec, a security-software vendor, about nine-tenths of the 140 billion emails sent daily are spam (unsolicited bulk commercial emails); of these about 16% contain money-making scams including phishing attacks[4]. E-mail fraud relies on naïve individuals who put their confidence in 'get-rich-quick' schemes such as 'too-good- to-be-true' investments or offers to sell popular items at 'impossibly low' prices. In this, confidence tricks tend to exploit the inherent greed and dishonesty of their victims: the prospect of a 'bargain' or 'something for nothing' can be very tempting. Over the years; email has evolved from a means of easy communication to one of the cornerstones of a large-scale criminal economy. For example, Spam today is best known as a way to steal a person's identity and sensitive data or to gain access to corporate intellectual property and used as phishing[5]. The spam emails are often sent from Internet cafes equipped with satellite Internet at a very low cost. They consume significant resources of targeted computer and are used as a delivery mechanism for cyber-attacks. Spam often contains viruses, worms, scams, and drive-by download malwares. Symantec reports that 91.9% of email traffic is spam and that 95% of all spam is generated by botnets (i.e., malware infected remotely controlled computers)[6]. It may be noted that by opening spam, users open their machines and their entire network to become members of a botnet, which can compromise the entire network.

Phishing, is a variation on "fishing", " the idea being that bait is thrown out with the hopes that while most will ignore the bait, some will be tempted into biting"[7]. It is the act of attempting to fraudulently acquire sensitive information by masquerading as a trustworthy person or business with a real need for such information in a seemingly official electronic notification or message (most often an email, or an instant message)[8]. Phishing may lead to identity theft and fraud by finding out the users' personally identifiable information (PIIs) such as user name, passwords and credit card details typically for an economic gain by masquerading as a trustworthy entity in an electronic communication; such as pretending to be from a well-known organization, a legitimate online retailer, trustworthy companies, bank, government agency or someone claiming to be a prospective employer. Some phishing emails try to convince that something good will come from participation. More commonly, phishing attacks use email or malicious web sites to solicit personal, often financial information. Clicking a link in a phishing email typically takes one to fake website that may be related to even a scareware website. Common methods of installing malware in phishing attacks are carried out through fake advertisements or 'popup' windows on web sites. Experts suggest not clicking on links directly from a suspicious e-mail. Similarly, it may be mentioned that secure web sites use a technique called SSL (Secure Socket Layer), indicated by HTTPS:// instead of HTTP:// at the beginning of the address (the "S" stands for "Secure") and by a locked padlock icon which must be found either at the address bar or in the bottom right hand corner of browser window. A padlock appearing anywhere else on the page does not represent a secure site. It is also suggested if the first part of the web address consists of numbers; the site should probably not be trusted. Phishing attacks usually use a combination of email spoofing and web spoofing to trick people into giving personal and financial information. In particular, phishing and pharming (luring people to disclose sensitive information by using bogus emails and websites) are two popular security threats that netizens and financial institutions are facing at large. Pharming is a hacker's attack aiming to redirect a website's traffic to a bogus website where they harvest the users' information[9]. Pharming can be conducted either by changing the hosts file on a victim's computer or by exploitation of a vulnerability in DNS server software.

An added threat in new millennium is the recognition of internet as a useful tool by scammers/con artists, using hypnosis as a tool to make money by exploiting various

human weaknesses and emotional vulnerabilities. Hypnotizing people through the internet has a greater range. It allows the scammers / con artists to manipulate the victim's mind and play with it like revealing something that he / she doesn't want to reveal or making him / her to do something else. Given email's nature of human to human communications, it is being used as a social engineering vehicle by con artists/scammers. It is observed that many of the cyber-crimes related to data theft and identity theft display a judicious mix of cyber hypnotism and malwares. Recognizing the convergence of cyberspace and hypnotism, the author has used cyber hypnotism as a basket term for the type of scams and frauds, referred as crimes of persuasion, popularly known as London scams, Nigerian fraud, Canadian fraud, Romance scam, Lottery scam etc. These are scams that appeal to people's greed, goodwill or other emotions to use the victim to provide the access and assistance to information, the money or other resources, that are the target of the criminal. What is common in all these scams is that scanned versions of official documents are emailed to potential victims in order to convince the genuineness of the transaction. Internet users, now, need to be more vigilant as new and more insidious mind tricks arise every day, especially if a message is either too good or too bad to be true. Users are too often seduced by a wonderful offer or alert. It is suggested to be suspicious if someone contacts unexpectedly and asks for personal information. Appeals to achieve happiness via increased wealth, relationships or health are tempting people to become scapegoat. It is noted that if the message appears to be one of gain then promotion-focused individuals tend to be motivated and get attracted to go ahead, whereas others who are prevention-focused individuals, tend to be motivated to avoid the sky falling i.e., heavy losses. Both types of individuals are illusioned by legitimacy and/or associated with such messages. In cyberspace, for instance, in order to convince the legitimacy of the email, all publicly available highly-personalized information is included by scammers/con artists in such emails. Furthermore, they create a story line in such a way that it induces the emotional sensitivity of the innocent human beings, and then they ask either for wire transferring the money or provide a website link within an email, which serves many purposes. For example, the link may be relating to a login page of any financial institution so as to get the PIIs from the legitimate users, resulting not only in the theft of login information but also in the identity theft as well as credit card fraud. The link may be relating to a login page of any email account like Gmail, Yahoo, RediffMail etc. where the user enters his / her login information and unknowingly helps the con artists in delivering his / her secret credentials. Afterwards, the scammer / con artist may use the contacts present in the address book and will try to scam other people from the contacts. Similarly, the link may be related to a legitimate website embedded with blended malware which makes the website visitors' machines a cyber- victim. However, this remains hidden from the first-owner of the computer system. By this way, the scammer/con artist creates a backdoor in the computer system and is able to monitor and control the computer system remotely. This information is generally sold in the underground market of internet. All such incidents are happening because people are hypnotized to such an extent that they are ready to believe what the scammers / con artists are trying to convey. Furthermore, a widespread use of commodity operating systems and software products delivering rich functionality but lacking security has aggravated the problem.

Investigation of cyber- crime cases and appraisal of threat data analyses of online crimes especially related to cyber hypnotism reveals that many of these are being carried out with basic equipment and a simple scheme with little efforts. Hence, contrary to popular belief, most of such attacks perpetrated against computer systems do not require a high level of technical sophistication, yet present an unprecedented challenge for law enforcement authorities. As technologies become more user-friendly, computer-users require less computer knowledge and are, therefore, more vulnerable to cyber-crime, home users perhaps the most. Often poorly protected, personal computers are a favorite target for such criminals.

3. CYBER VIGILANTISM: A DISCUSSION

McAfee reports a 660% rise in scareware over the past two years, and a 400% increase in reported incidents in 12 months. It also reports that cybercriminals make profits upwards of $300 million worldwide from scamming consumers with scareware [10]. A study conducted by U.K. Government in February 2011 on the cost of cyber-crime reports that U.K. citizens are losing £ 30m due to scareware and fake anti-virus[11]. Furthermore, it is a rgued that fake anti-virus software operation generate many millions of dollars and investing this dirty money into Internet Service Providers (ISPs) for shady dealings is also emerging as a very sensible move for bad guys. ISP's are often accused of not doing enough to police illegal traffic. In order to curb scareware, it is felt that anti-virus deployment in computer systems must be made mandatory while hiring an internet connection from ISPs or their vendors, which may be audited by ISP's at the time of providing internet services to their potential customers and may be counterchecked by cyber vigilantes. It is observed that cyber criminals are increasingly using highly reputable and popular legitimate websites and social networking pages to infect computers.

Looking at such unprecedented challenges, the author strongly advocates a policy of involving high tech cyber security experts and encouraging cyber vigilantism with government as regulatory authority to co-ordinate them. During cyber-crime investigations, the exact nature and positioning of cyber-crime evidence can be crucial to unraveling the chain of events. Time stamps in logs, records of network activity, new directories and files created by the attacker, incoming /

outgoing mail or other packets during the period when the intruder was actively exploiting the system; all of these are important pieces of the overall puzzle. It is suggested that these professional cyber vigilantes can be utilized to gather such evidences. Cyber Vigilantism by private citizens is a response to their frustration with the number of rogue sites in operation and what they believe is the unwillingness or inability of our government to take them down. It is felt that conventional law enforcement just can't match the skills needed. Besides, one can't trust law enforcement to keep ones secrets from becoming public knowledge. It is worth to mention that after 9/11, it is self-styled vigilantes who came to America's rescue. Similarly, Cyber Vigilante Groups may be used as a source of information in the Figure1 against fraud, wherein consuming the bandwidth of fraudulent banking and lottery sites in an attempt to force them off the internet. It is learnt that few of the cyber vigilantes are open source cyber analysts who also visit extremist sites to glean information. One of the most famous examples of such Cyber Vigilante Groups is The Jester (th3j35t3r) who forces off Cyber Jihad websites[12]. They can offer advise and tools on how to avoid scammers and list suspected fraudulent websites. They can search logs of Internet service providers for "attack packets" and try to trace where they are coming from and who is behind them. They can also assist when businesses are faced with the first manifestations of cyber-crimes, such as threats besides educating internet users so that they take basic precautions when surfing the web. In addition, cyber vigilantes may also be utilized for website and domain ratings to benefit users. It is worth to record that most interesting action occurs behind the scenes, wherein security vendors, internet service providers, domain name registrars and some of the most talented individual researchers globally communicate every day on new attacks, compromises, bots and threats. Malware and exploit samples, locations of compromised hosts and information on crime ware are shared as quickly as the information is generated. Most importantly, these non-governmental people, many of them working for free, are all there working together as cyber vigilante to thwart various cyber threats. Such voluntary security professionals/academia take reports every day from the internet provide timely and actionable information on botnets and malware threats and also pass this information to the public.

4. SCAREWARE: FORENSIC RESEARCH METHODOLOGY

Scareware is malware masquerading as free or trial anti-virus software or some other free online scam[13]. In this context, the author while performing the routine activities in the month of July 2010 in Computer-Aided INvestigative Environment (CAINE), a Linux operating system that offers a complete forensic environment, received an email message of an international cyber security conference (Figure 1). Since the email was highly personalized, hence, the author thought it to be a benign one. It is noteworthy that the email was received in the inbox and not in the spam. It was containing a website link of the international conference's website. In order to know more about the theme and topics of the conference, the author clicked on the given link. The website too looked like a legitimate one. After few seconds, the author observed a pop-up alert with a warning message of privacy violations. It gave an impression as if a trial version of anti-virus software had scanned the system under reference but unable to clean these privacy violations. The popup alert also displayed the recommendation to purchase full version of the trial version to remove privacy violations (Figure. 2).

Figure 1: "CAINE Operating System Environment"

Figure 2: "Popup Alert"

After selecting 'Remove Now' option, an Antivirus XP Professional tool got downloaded, which revealed that the system is infected with serious threats displaying a full-screen image of My Computer's environment that always appear in Microsoft Windows XP, with a message to remove the Viruses and Trojans found in the system (Figure

3). The Windows Operating System typeface (a look similar to the 'My Computer' in Windows XP environment) raised an immediate suspicion for further investigation about its genuineness since the author was working in a Linux environment as shown in the Figure. 1. Hence, it was decided to carry out further investigation.

Evidently, the threat warning was a fake one probably a scareware (rogue anti-virus & anti-spyware program) attack. Usually, scareware sellers use popup advertisements deliberately designed to look legitimate using the same typefaces as Microsoft and other well-known software providers. They appear, often when the user is switching between websites, and falsely warn that a computer's security has been compromised. If users click on the popup message, they are directed towards another website where they can download the fake anti-virus software supposedly needed to clean up their computer.

Figure 3: "Fake Warning of Infection (AntiVirus XP Professional)"

After clicking on the "Remove All" in Figure. 3, a website opened having URL address as www.scan4you.biz, and IP address as '85.31.101.148' which was reverse mapped as '85.31.101.148.static.nano.lv' with the Route / AS as '85.31.96.0/21' / '43513'[14]. On further forensic analysis of the popup and the website, it was found that the image shown in the website was hosted at "http://i080.radikal.ru/1004/c9/760db777d446.jpg" (Figure. 4).

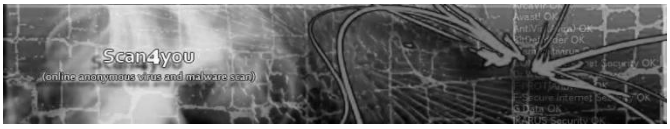

Figure 4: "Image of Website from where Scareware was downloaded"

On clicking the 'Buy Now' button shown in the website, a fraudulent payment page opened asking for all PIIs as well as financial information (viz. username, password for login into the anti-virus account, email id, credit card number, PIN number, issue/expiry date, full name of the card holder). Further details of the payment page are given in Table 1.

URL of Payment	4-open-davinci.com
Hosted IP Address	92.241.177.188
ISP	OAO Webalta
Location	Yoshkar-ola, Russia

Table 1: "Fraudulent Payment Page Details"

Instead of providing the information on the fraudulent payment website, the author registered the scareware by reverse engineering the downloaded malicious tool for further investigation in Windows XP environment. After installation, at the very first instant following major changes were observed:

1. Task Manager was disabled
2. Malfunctioning of [Ctrl] + [Alt] + [Delete] command
3. 'Folder Options' disabled
4. New registries were created, and the existing ones were modified

Default start page, & default search engine of Internet Browsers were changed to www.lameplaying.com/index.php/database.

Furthermore, following files were being created in each and every folder with hidden attribute selected by default:

1. tsjgiq.exe
2. khx <no extension>
3. khy <no extension>
4. <foldername>.EXE i.e., copy of each folder with an extension of .EXE

Apparently, all the above files were using rootkit technique. A rootkit is software that enables continued privileged access to a computer while actively hiding its presence from administrators by subverting standard operating system functionality or other applications[15]. It may be noted that once a rootkit is installed, it allows an attacker to mask the ongoing intrusion and maintain privileged access to the computer by circumventing normal authentication and authorization mechanisms.

Later on entering the URL of Gmail.com in Mozilla Firefox web browser, it opened a website www.lameplaying.com/index.php/database (IP address: 67.215.65.132) demonstrating possibility of Pharming.

Furthermore, network forensic was carried out by installing an Intrusion Detection and Prevention System (IDPS) in order to monitor the network activities, supposedly being carried out after the installation of scareware. It indicated that the scareware was continuously sending packets with variable size (in bytes) to an IP address with following log analysis data (Table 2).

Hosted IP Address	92.241.190.172
Company / ISP	Heihachi Ltd. / OAO Webalta
Location	Moscow, Russia

Table 2: "Details of Scareware to external IP Address"

It is noteworthy that although an internet connection of 2 Mbps (= 2,048 Kbps) was being used, there was a significant change in the network bandwidth before and after the installation of scareware that can be populated as in Table 3 and Table 4, respectively.

Ping	Download	Upload	Total Bandwidth
34 ms	512 Kbps	460.8 Kbps	2048 Kbps

Table 3: "Before installation of scareware"

Ping	Download	Upload	Total Bandwidth
96 ms	32 Kbps	8 Kbps	2048 Kbps

Table 4: "After installation of scareware"

Network forensic on the packet captured and the log files obtained from IDPS revealed that multiple requests and information were being sent as given in Table 5.

IDPS logs indicated port ranges between 1888 & 2132. Furthermore, for the IP address 77.91.227.248:2129, the remote system's MAC ID (i.e., machine address) was found to be 00-19- E0-A0-B2-8E. A route map of jebena.ananikolic.su is given in Figure. 5.

Protocol / URL	Port No.	Country	IP Address
jebena. ananikolic.su	2129	Moscow, Russia	77.91.227.248
UDP	2132	Moscow, Russia	92.241.190.130
UDP	2132	Moscow, Russia	92.241.190.172
UDP	2132	Moscow, Russia	92.241.190..237
UDP	1888	Brno, Czech Republic	89.102.0.150
http://search alligator.com/	80	Bellevue, US	8.5.1.41

Table 5: "Details obtained from network forensic"

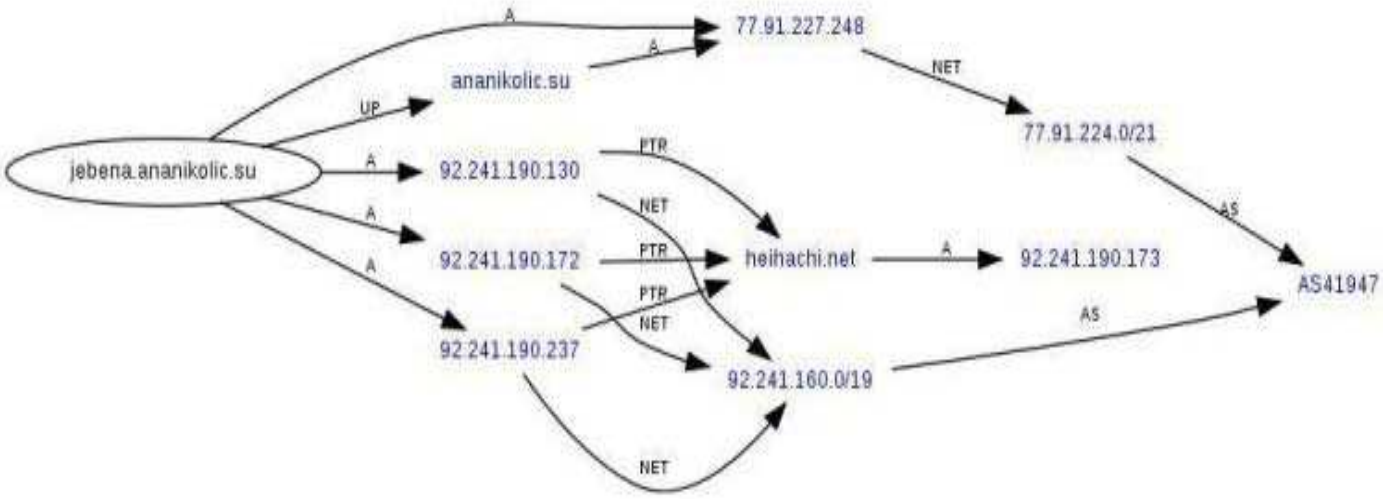

Figure 5: "Route Map of jebena.ananikolic.su"

Additionally, when the scareware was run in a network environment, there were multiple PING requests being relayed with payload (Table 6).

Protocol	Port No.	Request Type	Information
ICMP	6	Type 8 (Echo Request)	BOOTPS DHCP Server
SSDP	190		239.255.255.250

Table 6: "Scareware in a Networking Environment"

On further investigation, it was revealed that by using IPNAT (IP Network Address Translator) a request list was being sent at a very short but regular interval to the Russian IP addresses containing following parameters:

1. Subnet mask
2. Domain name
3. Router
4. Domain Name Server

Finally, the source file was located which was functioning as scareware having following aliases. Interestingly, these aliases were changing their names after every reboot randomly from the following ones:

NEBIH.EXE	:	141,824 bytes
RMHZB.EXE	:	138,752 bytes
1412294.EXE	:	140,800 bytes
86221.EXE	:	133,120 bytes
73911852.EXE	:	size was varying after every click

After performing intensive malware forensic, some very interesting information was uncovered. These were:

(1) Shell Command of Scareware:

```
shell\\\open\\\command=VEROVALA\\\\\nebih.exe
shellexecute=VEROVALA\\\\\nebih.exe
shell\\\explore\\\command=VEROVALA\\\\\nebih.exe
icon=SHELL32.dll, 4
open=VEROVALA\\\\\nebih.exe
USE AUTOPLAY=1
```

Figure 6: "Scareware shell command"

Here, the command icon=SHELL32.dll, 4 as shown in Figure. 6 was actually trying to conceal its icon as shown in number 4 (Figure. 7):

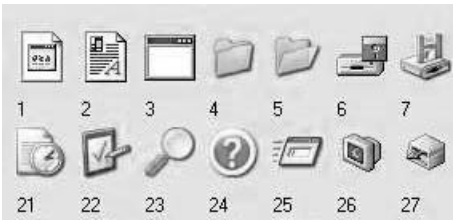

Figure 7: "SHELL32.dll icon graphics codes"

(2) MD5 hash value of NEBIH.EXE is as under 04509f3c5ef5b90a7addc09e65454fcc350745a39

(3) Following website links were found:
   1. www.egydown.com (website for Cracked software),
   2. www.filestube.com (malicious search engine),
   3. www.thepiratebay.org (torrent website),
   4. jebena.ananikolic.su (pornographic contents)

(4) Additionally, an encrypted HTML file was also revealed on the following path: C:\Documents and Settings\<username>\local settings\temp\cfircyh => HTML.Crypted!IK
It appears that to avoid detection by antivirus software, authors of HTML.Crypted!IK malware use browser features like JavaScript and VisualBasic Script. These scripts are small and very often quite simple encryption routines hiding the malicious parts of the script. Till date, the author isn't able to decrypt the HTML file.

(5) VEROVALA and NEBIH.EXE was showing a unique behavior in that it was using the same file icon as the antivirus software installed in the system under reference. Perhaps, it was done in order to fool those victims / users who just click on the icon but never read the full filename (with extension). As soon as any Plug-and-Play (UPnP) device was inserted, this file used to copy itself into it with the hidden attribute selected by default.

(6) Behavioral Pattern of VEROVALA / NEBIH.EXE: The registry values added to the system as soon as the USB drive is inserted were:
   1. HKEY_USERS\.DEFAULT\Software\Microsoft\Windows\CurrentVersion\Explorer\Advanced|Hidden
   2. HKEY_USERS\S-1-5-21-4058357071-1071901202-2123665184-1000\Software\Microsoft\Windows\CurrentVersion\Explorer\Advanced|Hidden
   3. HKEY_USERS\S-1-5-18\Software\Microsoft\Windows\CurrentVersion\Explorer\Advanced|Hidden
   4. HKEY_USERS\.DEFAULT\Software\Microsoft\Windows\CurrentVersion\Explorer\Advanced|Hidden
   5. HKEY_USERS\S-1-5-21-4058357071-1071901202-2123665184-1000\Software\Microsoft\Windows\CurrentVersion\Explorer\Advanced|Hidden
   6. HKEY_USERS\S-1-5-18\Software\Microsoft\Windows\CurrentVersion\Explorer\Advanced|Hidden
   7. HKEY_USERS\S-1-5-21-4058357071-1071901202-2123665184-1000\Software\Microsoft\Internet Explorer\Main|Default_Search_URL
   8. HKEY_USERS\S-1-5-21-4058357071-1071901202-2123665184-1000\Software\Microsoft\Internet Explorer\Main|Search Page
   9. HKEY_USERS\S-1-5-21-4058357071-1071901202-2123665184-1000\Software\Microsoft\Internet Explorer\Search_Assistant
   10. HKEY_LOCAL_MACHINE\Software\Microsoft\Internet Explorer\Main|Start page

(7) RMHZB.EXE created following registry keys:
   1. \Registry\Machine\Software\Microsoft\Windows NT\CurrentVersion\Winlogon
   2. C:\documents and settings\<username>\application data
   3. My Computer\HKEY_LOCAL_MACHINE\Software\Microsoft\WindowsNT\CurrentVersion\Winlogon\Taskman

(8) RMHZB.EXE and NEBIH.EXE is seen to perform following behavior:
   1. Uses rootkit technologies to conceal its presence,

interrogation or removal.
2. Found on infected systems and resists interrogation by security products.
3. Has code inserted into its Virtual Memory space by other programs.
4. Writes to another Process's Virtual Memory (Process Hijacking)
5. Created as a Process on Disk.
6. This Process deletes other processes from disk.
7. Crashing down the computer terminals arbitrarily.

Currently, a number of digital tampering detection techniques are available [16]. Interestingly, for further confirmation when author contacted www.virscan.org on 25th September, 2010 and submitted sample of NEBIH.EXE the result was astonishing. Out of 35 malware scanners existing on the website none was able to show that its' a scareware or a malware. Everyone showed it as a clean file. However, on 27th September, 2010 when author again contacted the abovementioned website, the result was that 11% i.e., 4 out of 35 scanners found it as a malware[16].

5. SCAREWARE: IMPLICATIONS

Tracking digital footprints of scareware samples under study indicate that a Denial of Service (DoS) attack using the Universal Plug and Play (UPnP) NOTIFY directive can be carried out by sending a malicious UDP packet to port 1900 containing a Simple Service Directory Protocol (SSDP) advertisement. An attacker can force the Windows client to connect back to a specified IP address and pass on a specified Hypertext Transfer Protocol (HTTP) or Hypertext Transfer Protocol Secure (HTTPS) request. If the system that the victim is attempting to contact for the device description is configured to "echo" such requests, the system will enter an infinite download loop that will quickly consume the system's resources and cause it to crash. It may be mentioned that denial of service is considered as one of the most difficult attacks to detect [18].

Additionally, a distributed denial of service (DDoS) attack using the UPnP NOTIFY directive can also be launched. It is similar to the first exploit, except the attacker sends the SSDP announcement to broadcast addresses and multicast. Multiple machines reply to the IP address to obtain the device description performing a DDoS attack against the system. This was seen when author tested the scareware in a networking environment where multiple systems are connected to the Internet.

6. CONCLUDING REMARKS

Malware is widely available on the internet for anyone wanting to cause mischief, theft, espionage or cyber-crime. The majority of internet users worldwide have fallen victim and they feel incredibly powerless against faceless cyber criminals. The fundamental issue is that there is a law enforcement model that's geographically based, but there's no geography on the internet. An in-depth data analysis of crimes of persuasion including the case study under reference demonstrates that many of the popular cyber-crimes are related to data theft and identity theft and display a judicious mix of cyber hypnotism and malwares. Such crimes can be handled, to a large extent, with constant vigilance at individual level in combination with safe security practices including deployment of malware threat mitigation controls. On the contrary, sophisticated cyber-attack in the form of scareware demands a better and more coordinated strategy on national level, which is required to be implemented by developing a suitable corporate defense plan including involvement of cyber vigilantes to ensure stronger cyber security. It is evident from present study that in such a scenario, when the branded and reputed anti-virus/anti-spyware vendors are unable to detect such well-crafted and encrypted malware planted by the clever but malicious entrepreneurs, the common man is left with no choice. Neither the local law enforcement agencies are equipped to cater the victim's need, nor the government with their policies. Furthermore, the scareware scam is hard for police or other law enforcement agencies to investigate because the individual sums of money involved are minuscule. Nonetheless, these cyber criminals strike time and again. Hence, the author advocates that to discourage criminals and to instill faith in the digital medium at large, there is an urgent need to coordinate all cyber vigilantes. Undoubtedly, proactive security is need of hour wherein the central government may act as a regulatory authority for these cyber vigilantes' supposedly high tech cyber security experts, who, in coordination, may prove valuable assets to safeguard the national economy in an unsafe cyberspace and to disseminate knowledge and information related to it.

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Boosting Geographic Information System's Performance using In-Memory Data Grid

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Abstract - A typical Geographic Information System(GIS) is information system that integrates, stores, edits, analyzes, shares and displays geographic information for effective decision making. The focus here is to refine the storing and retrieving capabilities of any GIS. GIS application have a very high performance and scalability requirement, such as query response time of less than 3 seconds, 120000 customer sessions per hour and 100000 data addition/updates per day. Also an ideal GIS application always deal with high concurrent load, frequent database access for mostly read only data, and non-linear growth of mostly read only data over period of time. These all are the factors which lead to performance impact in the application. This research proceeds to understand how the In-Memory Data-Grid solution is better than other solutions and how can it be leveraged to implement a very high performing and highly scalable GIS applications.

Index Terms - ***In-memory data grid, Cache memory, Geographic Information system (GIS), Distributed cache***

1. INTRODUCTION

Geographic Information system, commonly known as GIS is a computer system capable of capturing, storing, analyzing, and displaying geographically referenced information, that is, data identified according to location. Practitioners also define a GIS as including the procedures, operating personnel, and spatial data that go into the system.

A GIS application[7] requires low response time, very high throughput, predictable scalability, continuous availability and information reliability which can be provided by In-Memory Data Grid.

In-Memory Data Grid is a Data Grid that stores the information in memory in order to achieve very high performance, and uses redundancy - by keeping copies of that information synchronized across multiple servers in order to ensure the resiliency of the system and the availability of the data in the event of server failure[5].

Over the last few years, In-Memory Data Grids have become an increasingly popular way to solve many of the problems related to performance and scalability, while improving availability of the system at the same time. In-Memory Data Grid allows eliminating *single points of failure* and *single points of bottleneck* in the application by distributing the application's objects and related processing across multiple physical servers.

One of the easiest way to improve application's performance is to bring data closer to the application, and keep it in a format that the application can consume more easily.

Most enterprise applications are written in one of the object-oriented languages, such as Java or C#, while most data is stored in relational databases, such as Oracle, MySql or SQL Server. This means that in order to use the data, the application needs to load it from the database and convert it into objects. Because of the impedance mismatch between tabular data in the database and objects in memory, this conversion process is not always simple and introduces some overhead, even when sophisticated O-R mapping tools, such as Hibernate or Eclipse Link are used.

Caching objects in the application tier minimizes this performance overhead by avoiding un-necessary trips to the database and data conversion. This is why all production-quality O-R mapping tools cache objects internally and short-circuits object lookups by returning cached instances instead, whenever possible.

2. PROBLEM STATEMENT

2.1 Introduction to the Problem

Customer expectations from GIS systems have evolved significantly over a period of time [4]. Today customers are expecting better and faster online experience.

Several architectures are proposed to retrieve necessary, interested and effective information efficiently and at the same time provide scalable platform for GIS application. However, the results of these architectures generally become unsatisfactory and prone to performance loss over the period of time. As soon as the customer base increases, the performance starts retarding.

3. PROPOSED SYSTEM

The proposed system is trying to inculcate the technology called distributed cache in a GIS application. This technology will not only boost performance of application but will also provide many more features to it. The first step in our paper is a strong research base of prevalent architectures and secondly an in-depth study of distributed cache technology . After the research we will try to prove our concept through a small proof of concept.

If we are able to incorporate distributed cache in an GIS application the following feature would be achieved

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1. Low response time
2. High throughput
3. Eliminate bottlenecks
4. Predictable scalability
5. Continuous availability
6. Failover support
7. Information Reliability

4. LITERATURE REVIEW

Simple database retrieval architecture is still the back bone for most of the complex architectures in use today [8]**.** GIS application generally contains a program running on server, and is connected to a database. Numbers of users are connected to this program to query, update, delete or add different items.

Initially, application was deployed on a server which originally supports 5000(say) users at a time, which means that at a time 5000 users could connect to the server. No matter, how powerful a server was, for sure it would have some limit on number of users it could support, and therefore as an example here we have assumed that server could support 5000 users at a time.

There is further limit on number of users, whose requests required access to database that could be processed simultaneously. The reason behind this was that, connections created to database were generally heavy, as many connections to database at the same time were not feasible. To efficiently use connections to access to database, developers generally used connection pools, and set a limit on number of connections that could be active at a time. Other then performance issues the other issues regarding the architecture were:

4.1. POF, which stands for single point of failures. In the architecture there were three single points of failures: application, database and server. In case either database crashes or server crashes or application crashes, complete application would be down and no one would be able to access the application or use application.

4.2. Shared resources were always performance bottlenecks and greater the number of connections/users a shared resource would have more will be the affect on performance. Whereas in the previous architecture, database was a shared resource, which could not support large amount of users at same time.

4.3. Another reason of low performance with the basic architecture was the step required to convert data stored in database to application object, when user queries for data stored in database, and step required reading application object to store data in database.

To take care of number of users supported by application, load balancer was introduced [2]. Load balancer's responsibility is to distribute the load efficiently among different servers/applications capable of process the request. In this architecture load balancer application is run on one system and GIS application is deployed and run on more than one server which is further connects to single database. Load balancer forwards the user requests to any of the server configured with load balancer based on the load of the server. The use of load balancer tremendously increased the number of users that could simultaneously connect to application, as number of servers running the application was increased. But there were still large performance issues with the architecture [9].

Still, there is limit on number of users whose requests required access to the database, the reason being limit on number of connections that could be made simultaneously to the database.

SPOF still existed. Though server running the application was no longer, single point of failure, as there were more servers which were present, which would be able to keep application running even if any server or application running on any server crashes. This would remain transparent to users, as users were no longer interacting with the server hosting the application, but users were interacting with the load balancer. When load balancer would get news of one of the server being down, it would then exclude that server from its list of active servers and stop delegating any of the user requests to that specific server. But database was still single point of failure, as we were using single database, and if that database would crash, the application would fail.

Cris J. Holdorph[3] gave an approach to work with distributed database instead of single database. In this scheme, it was considered that each server which was connected to a load balancer was having its own database.

Though, number of users which could be supported now increased, compared to above discussed schemes, but this scheme would require another extra process to replicate the data stored in one database to other databases. This was required to take care of scenario, when user requests were sent to different database. The result sent back should be consistent and independent of data stored on database.

Jim Handy[6] defined a scheme in which multiple servers were connected to single cache, which are further connected to the database.

The number of connections that could be made increased (though this number depends on the server on which cache is hosted). Also the read queries would be much faster, and performance of write queries to the database would be improved if the updates were done in cache synchronously, and asynchronously saved in database by some other process. But there were still some disadvantages related to this scheme like cache and database were still single point of failure, if any of it crashed, application would not be available. Data-intensive queries would run on complete data in cache, which was not very efficient.

In recent past there was a concept of In-Memory Data Grid and related products which have become famous, which could be used to improve performance of applications which are highly affected by database operations and mostly read only operations [8]. In GIS applications most of the requests are related to read-only requests which require reading something from database. Most of the users request sent to server are read-only request and insert/update command is used only when new point is located.

Paul Colmer[5] described the features provided by In-memory

Data grid, which makes it a good choice for GIS application. An In-Memory Data Grid achieves low response time for data access by keeping the information in-memory and in the application object form, and by sharing that information across multiple servers. In other words, applications may be able to access the information that they require without any data transformation step .

Performance is further improved by coalesces multiple changes to a single application object and batches multiple modified application objects into a single database transaction, meaning that a hundred different changes to each of a hundred different application objects could be persisted to a database in a single, large and thus highly efficient transaction[10].

Arindam Chakravorty[1] discussed various topologies in which cache could be used to overcome the limitations of above schemes**.** In-Memory Data Grid supports three types of caches. These are Distributed, Near and Replicated cache topology.

Distributed cache is one in which each node in the server contains a unique set of application data in the cache. To scale the capacity of cache, increase the nodes in the cluster. Any type of cache will involve serialization /de-serialization and network transfers for application data read and write access in the cache. Distributed cache is best when the applications requires heavy volume of read and write application data.

Distributed Cache architecture is shown in Figure 1.

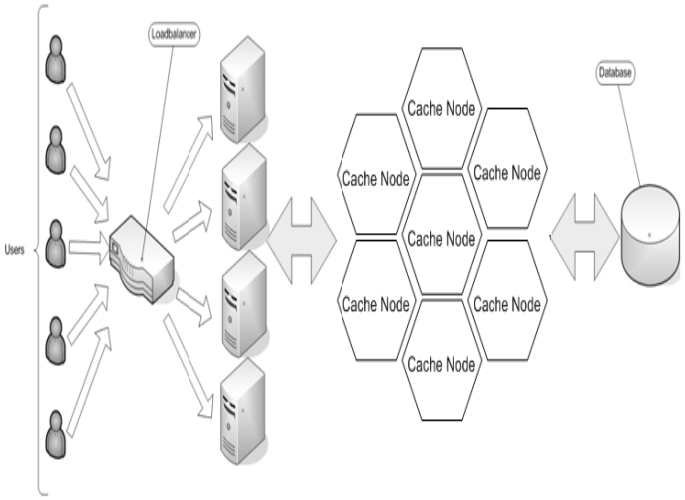

Figure 1: "Distributed Cache Architecture"

Near cache is each client node containing small amount of data in the local cache and larger amount of data in the distributed cache and these caches are synchronized with each other. There is some overhead involved with synchronizing the caches.

In Replicated cache each node in the cluster will contain all the application data in the cache. Replicated cache is best when application requires less application data and highly read access from cache.

5. GRID CLUSTER ARCHITECTURE

5.1 Grid Cluster Architecture

In-Memory Data Grids[8] are built on a fully *clustered* architecture. Grid is based on a peer-to-peer clustering protocol, in which servers are capable of:

5.1.1. **Speaking to Everyone:** When a party enters the conference room, it is able to speak to all other parties in a conference room.

5.1.2. **Listening:** Each party present in the conference room can hear messages that are intended for *everyone*, as well as messages that are intended for that particular party.

5.1.3. **Discovery:** Parties can only communicate by speaking and listening; there are no other senses. Using only these means, the parties must determine exactly who is in the conference room at any given time, and parties must detect when new parties enter the conference room.

5.1.4. **Working Groups and Private Conversations:** Although a party can talk to everyone, once a party is introduced to the other parties in the conference room (i.e. once discovery has completed), the party can communicate directly to any set of parties, or directly to an individual party.

5.1.5. **Death Detection:** Parties in the conference room must quickly detect when parties leave the conference room – or die.

Using the conference room model provides the following benefits:

1. There is no configuration required to add members to a cluster. Any program running grid application when starts will automatically join the cluster and be able to access the caches and other services provided by the cluster. When a program joins the cluster, it is called a *cluster node*, or alternatively, a *cluster member*.
2. Since all cluster members are known, it is possible to provide redundancy within the cluster, such that the death of any one node does not cause any data to be lost.
3. Since the death or departure of a cluster member is automatically and quickly detected, failover occurs very rapidly, and more importantly, it occurs transparently, which means that the application does not have to do any extra work to handle failover.
4. Since all cluster members are known, it is possible to load balance responsibilities across the cluster. Grid does this automatically by distributing the load evenly across cluster. Load balancing automatically occurs to respond to new members joining the cluster, or existing members leaving the cluster.

6. READ-THROUGH CACHING

When an application asks the cache for an entry, for example the key X, and X is not already in the cache, data grid will automatically delegate to the cache-store which is responsible for loading data into cache, and this cache-store will now load X from the underlying datasource.

If X exists in the datasource, the cache-store will load it, return it to data grid, which is then placed in the cache for future use and also data X is returned to the application code that requested it. This is called **Read-Through** caching.

7. WRITE-THROUGH CACHING

Coherence can handle updates to the datasource in two distinct ways, the first being Write-Through[2].

In this case, when the application updates a piece of data in the cache the operation will not complete (i.e. the put will not return) until data is also persisted to the underlying datasource. This does not improve write performance at all, since the user is still dealing with the latency of the write to the datasource[10].

8. REFRESH-AHEAD CACHING

In the Refresh-Ahead scenario, Coherence allows a developer to configure the cache to automatically and asynchronously reload (refresh) any recently accessed cache entry from the cache loader prior to its expiration.

The result is that once a frequently accessed entry has entered the cache, the application will not feel the impact of a read against a potentially slow cache store when the entry is reloaded due to expiration. The refresh-ahead time is configured as a percentage of the entry's expiration time; for instance, if specified as 0.75, an entry with a one minute expiration time that is accessed within fifteen seconds of its expiration will be scheduled for an asynchronous reload from the cache store.

9. WRITE BEHIND CACHING

In the Write-Behind scenario, modified cache entries are asynchronously written to the datasource after a configurable delay, whether after 10 seconds, 20 minutes, a day or even a week or longer.

For Write-Behind caching, grid generally maintains a write-behind queue or any data structure which stores the data that needs to be updated in the datasource. When the application updates X in the cache, X is added to the write-behind queue (if it isn't there already; otherwise, it is replaced), and after the specified write-behind delay data grid service will update the underlying datasource with the latest state of X.

Note that the write-behind delay is relative to the first of a series of modifications – in other words, the data in the datasource will never lag behind the cache by more than the write-behind delay.

The result is a "read-once and write at a configurable interval" (i.e. much less often) scenario. There are four main benefits to this type of architecture:

1. The application improves in performance, because the user does not have to wait for data to be written to the underlying datasource.
2. The application experiences drastically reduced database load: Since the amount of both read and write operations is reduced, so is the database load. The reads are reduced by caching, as with any other caching approach. The writes - which are typically much more expensive operations - are often reduced because multiple changes to the same object within the write-behind interval are "coalesced" and only written once to the underlying datasource ("write-coalescing"). Additionally, writes to multiple cache entries may be combined into a single database transaction.
3. The application is somewhat insulated from database failures: the Write-Behind feature can be configured in such a way that a write failure will result in the object being re-queued for write. If the data that the application is using is in the cache, the application can continue operation without the database being up.
4. Linear Scalability: For an application to handle more concurrent users you need only increase the number of nodes in the cluster; the effect on the database in terms of load can be tuned by increasing the write-behind interval.

10. STATISTICS FOR COMPARISON

10.1 Database and In-Memory Data Grid Performance

The comparison shows that when the data is stored conventionally in databases the processing speed is more as compared to when it is stored in cache. The results have been shown in figure 2 and figure 3.

11. CONCLUSION

An effective caching mechanism is the foundation of any distributed-computing architecture. The focus of this article was to understand the importance of caching in designing effective and efficient distributed architecture. In memory data grid method was finally implemented for the same. It has been observed that retrieval time of GIS application's data saved using in memory data grid method is much less as compared to when the data is saved using the conventional database storage method. Thus, the use of distributed cache technology for spatial data storage will boost the performance of GIS application.

FUTURE SCOPE

Object relational mapping is a way to bridge the impedance mismatch between object-oriented programming (OOP) and relational database management systems (RDBMS). Many commercial and open-source ORM implementations are becoming an integral part of the contemporary distributed architecture. ORM technologies are becoming part of the mainstream application design, adding a level of abstraction. Implementing ORM-level cache will improve the performance of a distributed system. Therefore, this method can be used to improve the performance of the GIS application. In future, the digitized data required for GIS application can be stored using proposed Triangular Pyramid Framework for Enhanced object relational vector data model[3] under the distributed cache environment using in memory data grid for better results.

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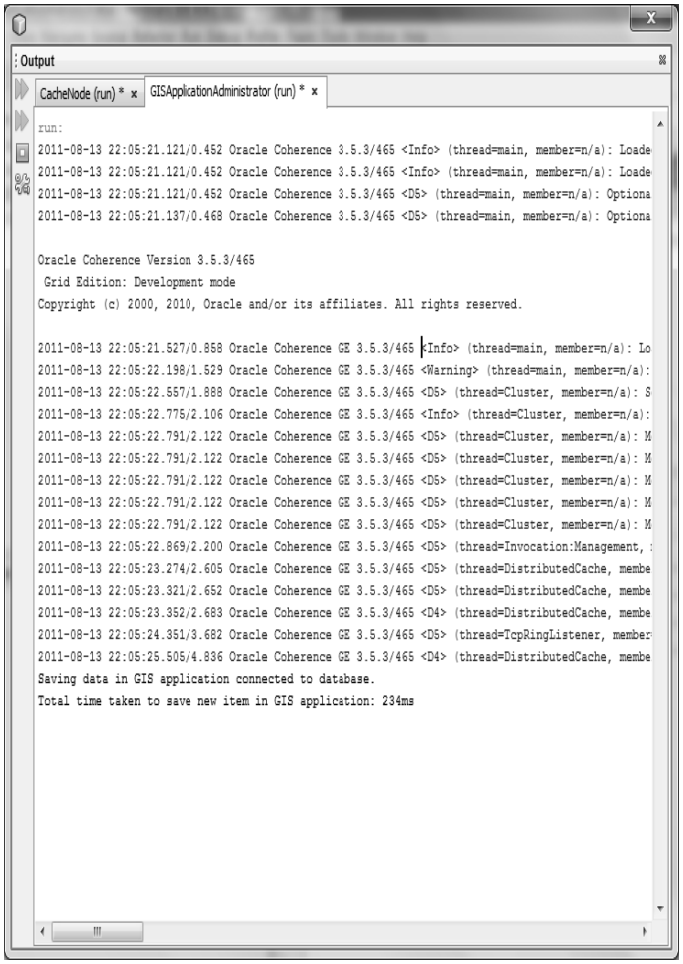

Figure 2: "Saving Item in Databases"

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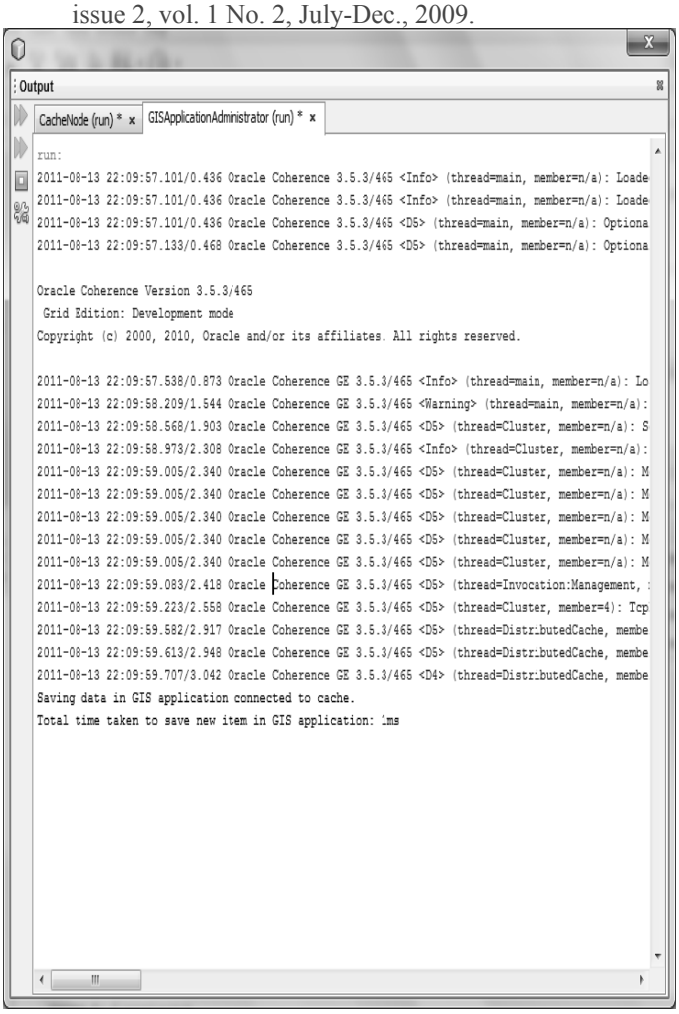

Figure 3: "Saving item in cache"

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Digital Communication and Knowledge Society

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Abstract - Knowledge is awareness at higher level of abstraction [5, 6, 7]. It has tacit and explicit components. Concern lies in conversion of tacit knowledge to explicit form and its scientific management since it is identified presently as an economic entity without diminishing return. Advancement in knowledge exercise contributes immensely towards socio-economic development of a community. This induces to explore ways to generate new scientific knowledge with evolving technologies. Communication is one approach of many alternatives to evolve new scientific knowledge through inter and intra entity data & information exchange. Data communication using digital technology in recent years has attained ubiquitous dimension and its affect on knowledge generation has grown enormously [3, 19], resulting in need for enhanced attention. Present text is an attempt in similar stratum.

Index Terms - Information Society, Knowledge, KAM-Knowledge Assessment Methodology, K4D-Knowledge For Development, KI-Knowledge Index, Knowledge Society, ICT-Information Communication Technology, IDI -ICT Development Index, Hyper Text, HTTP, TCP/IP.

1. INTRODUCTION

Civilization has surfed through agrarian, semi-industrialization, industrialization and advanced industrialization phases and arrived at information age where power has shifted from industrial to information and knowledge production and management leading to 'Information Society' concept wherein creation, distribution, and manipulation of information and knowledge has become the most significant economic and cultural activity [6,7].

Ahmad, Mazida [02] el al conveys, Nonaka and Takeuchi opines analyzing data from top Japanese industries that knowledge creation involves the processes of interaction and transaction of tacit and explicit knowledge between experts and novices that employ the processes of Socialization, Externalization, Combination, and Internalization (SECI).

There are different interpretations of knowledge. To have knowledge one needs to add value to data or information. This brings in the role of management in the entire process. As knowledge is awareness at higher level of abstraction, to acquire it institutionally collective business goal is to be on focus, which in turn calls for a mechanism to facilitate intra and inter entity fluent flow of data communication [6, 7, 8].

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The knowledge abstraction as depicted in figure1 is a process of awakening. The efficiency, with which it is attained, in terms of content and speed, varies amongst entities. In the figure, arrowed lines indicate flow of communication. Digital communication has become an important mode of knowledge exchange today. Comparatively, more knowledgeable institution or entity needs relatively lesser time and effort to traverse across information hierarchy, as depicted below in Fig-1 [6]. This requires skills for detailing, consolidation and communication. The speed and accuracy, with which an individual or an institution consolidates details to evolve knowledge, or traverse in reverse order from consolidation to detailing, reflects on its intelligence. The involved processes herein are both tangible and intangible in form.

Knowledge has both tacit and explicit components to deal with, making its management very fiddly. Exchange of thoughts, views and opinions through affective communication has always enhanced knowledge. The process of knowledge abstraction and its ramification at times is intangible and varies amongst entities or institutions. This makes tacit knowledge component bit inconceivable and its conversion to explicit form a challenge [4, 6].

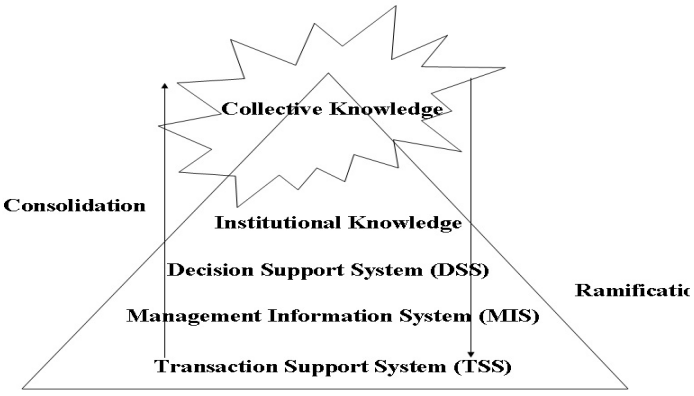

Figure1: "Institutional Intelligence System"

To avoid knowledge loss or distortion its tacit part needs to be communicated widely for better storage and editing on cognitive space through discourse, debates, discussion, and deliberation. Alternatively, its conversion to explicit form, in black and white or digital structure and communication over wide domain offers opportunity for future editing, up-gradation, retrieval and reuse. One may use either of the two techniques or both, in tandem. From time immemoriall, tools are being searched, used and improved upon to make it happen. Today ICT, amongst other available tools, with its power, agility and ubiquity provides one of the best options.

The issues on hand are to process data, information and knowledge and then share it on fast track. ICT works as a catalyst in this process, which has gone through evolution involving first, second, third, fourth and fifth generations of computing [1, 3]. This has made knowledge-generating practices to arrive on web1 to web2 and then on to web3 platform from standalone mode [21]. Exchange of thoughts and views over Internet worked as guiding force, framing public opinion in recent years, leading to notable changes in the social and socio-economic system. Recent upheaval in Middle East countries can be considered as case in point. Facebook, Twitter, Wiki etc are the platforms on Internet and World Wide Web where views and opinions are exchanged, edited and given shape by stake holders to evolve a collective perspective [26].
Discussions and deliberations on digital social network like ReseachGate are immensely popular amongst serious thinkers with strong research orientation. On ResearchGate, with over million members onboard and publications, covering various subjects from 'Mathematics' to 'Literature', knowledge gets generateds reviewed and updated online. This makes instant conversion of tacit knowledge to its explicit form possible. However, to be able to use these platforms effectively one needs to possess necessary ICT tools like a computer system and means to hook it on to a strong digital network [12].

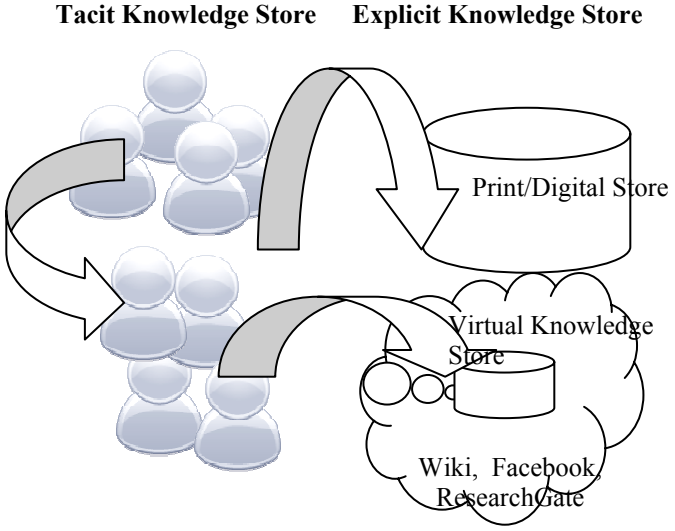

Figure2

2. KNOWLEDGE OBJECT WITH ICT AS AN ENABLER

From an abstract entity "Knowledge" in this era has evolved as an object with material and economic value, a fact recognized by international institutions. World Bank derived Knowledge and Knowledge Economic Index (KI & KEI) of counties considering 83 factors affecting their respective socio-economic conditions and ranked them according to the order during 2008 and 2009 [11]. According to these reports ICT is increasingly affecting socio-economic and cultural exercises leading to advanced knowledge.
IBM and Economic Intelligence Unit (EIU) are regularly publishing data on ICT preparedness of countries in the world and related ranking since year 2001 to 2009 [10].
In the year 2010, in keeping with changing scenario, it published digital economy raking of member countries [10, 15]. Recent report of International Telecommunication Union (ITU) [16, 17] of 2010 and 2011 on measuring information society concedes the role of ICT in enhancing socio-economic growth. It observes that if applied appropriately, ICT can be development enabler, critical to countries attempting to transform itself as a knowledge society.
Evolving computing and communicating techniques have affected Human-Computer relationship at various stages, which opened new avenues for knowledge generation. In the following section these aspects are briefly touched upon.

3. COMPUTING

The first generation computers of 1940-56 era used vacuum tubes for circuitry and magnetic drum for memory. Programming was done using machine language. Transistors replaced vacuum tubes in second-generation computers during 1956-63. For programming, Assembly Language was used on such computers. High-level languages like FORTRAN and COBOL were developed during this time to make usages easier. Miniaturized transistors, called semiconductors, which were placed on silicon chips ushered era of third generation computers during 1964-71. Use of semiconductors helped in radical enhancement of computing speed. Forth generation computers came into existence from 1971 with the arrival of microprocessors and are still in use, which also brought in GUI features, mouse and handheld devices [24]. Evolvement of various technical standards of computing enabled collaboration between technologies, pushing the growth faster. Fifth generation computers involving quantum computing and nanotechnology are in course of evolution. These efforts stepped up speed, efficiency and volume of information processing and at the same time elevated the quality of the process involved in information dispensation [19, 24].

4. COMMUNICATING

Evolution of Internet started in the 1950s and 1960s along with the development of computers. Initially this was to facilitate point-to-point communication between mainframe computers and their access points or nodes or terminals. Later it expanded to aid connections between computers leading to early research into packet switching. During 1970 Donald Davies developed a packet switched network called Mark I to support NPL (National Physical Laboratory). This was later, improved to Mark II in 1973 and it remained in operation till 1983. 'Larry Roberts' of 'Advanced Research Project Agency' in the United States took ahead the technology to ARPANET, which later evolved to INTERNET. In 1982 Internet Protocol Suite TCP/IP was standardized and concept of World Wide Network over TCP/IP came into existence. Berners Lee evolved world

information medium during 1990. He built all necessary tools for working on web, like Hyper Text Transfer Protocol (HTTP), Hyper Text Mark-up Language (HTML) and the first web browser (World Wide Web). At this instance during 1980-1990 commercial Internet Service Providers (ISPs) emerged [22, 23].

Efforts on standardization of computing and communicating practices increasingly become momentous from this occasion allowing diffusion of computer and communication technology in to all aspects of human life ranging from culture to commerce through fast exchange of data, information and message [15, 19 22].

Mark Weiser conceived the phenomena of existence of computing in every aspect of human life without any conscious reference and coined the word 'ubiquitous computing '. In one of his articles in "Scientific American" during 1991 he expressed that all profound technologies will be very much in common place and be taken for granted so much so that all will get oblivion to their existence. Later, ubiquitous computing and related fields like wearable computing and augmented reality, have become one of the major emerging areas of HCI research [28, 29].

5. PARADIGM SHIFT IN HUMAN VS COMPUTER RELATIONS

Electronic computing with Mainframe System had multiple users sharing centralized computing facility giving 'one computer to many user' relationship. Developments of microprocessors enabled creation of personnel computers leading to 'one computer to one user' relationship where each user possessed one computer to execute specific personal tasks. Evolution of TCP/IP protocol standard enabled to connect personal computers over digital network helping real time information sharing. The paradigm shifted further at the advent of Internet and World Wide Web, which allowed interconnection of computers across the world over Internet leading to 'one user many computer' environment. Evolution of standards and protocols contributed immensely in these efforts.

Miniaturization of microprocessors enabled embedded computing ability on various devices of day-to-day use leading to ubiquitous computing paradigm [03, 28, 29]. This made computers to have invaded in every aspect of life. To take things further ahead, virtualization and cloud computing emerged with offerings like Software (SaaS), Infrastructure (IaaS) and Platform (PaaS) as service to shape paradigm shift of computing to forth generation and beyond [8,12]. These facts encouraged computer and Internet usages reducing individual resource liability.

6. KNOWLEDGE GENERATION ON VIRTUAL PLANE

'Data communication' and 'Text Transfer' protocols like (TCP/IP) and (HTTP) paved path for INTERNET and World Wide Web (www) leading to Web1, Web2 and Web3 paradigm on which knowledge generation and exchange has become faster and simpler [21]. Standards and Protocols combined with advanced computing and networking features extended human reach and capability to express over virtual plane beyond defined spatial boundaries and media restrictions [01, 18, 26]. Web1 paradigm allowed us to create simple black and white static pages while Web2 allowed to be colorful with dynamic content. Web3 environment provides interactive web pages on which a piece of text can be created, edited or commented on instantly to have tacit knowledge converted in explicit form [21]. Computing capability and techniques over Web 2.0 & 3.0 are emerging as a very effective tool to process data and retain information to create Knowledge instantly online [08, 18, 19, 21]. This comes handy in registering tacit knowledge in explicit form too.

To take things further ahead, virtualization and cloud computing techniques are attempting to make advanced computing resources ubiquitously available without involving end users in the complexities of information storage and retrieval process. Leading ICT institutions and service providers like Oracle, IBM, Microsoft, Goggle etc. are coming up with virtualization and cloud computing options. Wikis, Blogs, Social Networking over digital platform etc. are modern day's podium for knowledge collaboration, tacit knowledge registration and up-gradation [12,18].

7. VIRTUAL ENTERPRISING

To remain competitive we need to identify what helps us best to traverse on the path of wisdom as shown in fig -1. Hendricks [14] opines that Information and Communication Technology (ICT) with Hardware equipments and software solutions can enhance knowledge sharing by lowering temporal and spatial barriers between knowledge workers, thus improving access to information on knowledge. He throws light on differential effects of ICT on the motivation for knowledge sharing in different settings. It is also observed that most successful companies are those who use their intangible assets faster and better.

Christian Kreutz [27] the founder of Crisscrossed indicated that Tagging (Marking), Social Book Marking (Networking), Blogging (Story Telling), Wikis the white board and RSS Feed are five tools for present day's knowledge sharing. For which one simply need to possess computing systems and access to Internet. This leads to the conviction that the overall structure for handling data and information presently is capable of accommodating more abstract inputs in business decision making process to enhance cognitive level at one end and its quick ramification leading to detail functional directions for effective business process execution on the other. This leads to the assurance that ICT facilitates 'knowledge production' with reasonable ease and effect can be seen in enterprise level conceptualization. '

'Enterprise 2' is the new buzzword where concept of social business is being consolidated. Enterprise 2.0 uses web 2.0 within organization to enhance collaboration leading to streamlining of business processes. "Enterprise 2.0" concept

was coined by Harvard Business School professor Andrew McAfee in 2006 to portray how the Web 2.0 "technologies could be used in organization's intranet and extranets. It is obvious now that in this era of collaboration, connectivity over data communication network holds the key [19, 21, 25, 26].
This necessitates assessing ICT strength in general and communication network in terms of broad band connectivity in particular to comprehend state of knowledge society. Today E-Readiness ranks and Broad band connectivity statistics indicates accessibility to ICT, one of the modern platforms of knowledge exercise.

8. ANALYSIS

At this instance assessment of Knowledge and Communication capability appears imperative. Country wise measures to assess Knowledge and Communication strength are brought in focus to analyze and comment on the context in the following section.

8.1 Connectivity

The report of International Telecommunication Union (ITU) [16, 17] of 2010 and 2011 on measuring information society, the concept as discussed in section 3 of present text, finds the touchable role of ICT in enhancing economic growth and socio-economic development
It observes that if applied appropriately, ICT can be development enabler, critical to attempting to transform countries as a knowledge society and the concept is pivotal to the measure IDI (ICT Development Index). According to the report, apart from productivity, ICT impacts other economic and socio-economic factors like digital inclusion, access to knowledge and information, acquisition of skills increasingly in demanded in a range of occupations and even in school performance. It considers availability of infrastructure, access and effective use, with skill and intensity forms the core context, which has an impact on knowledge society. ITU member states are considering ICT demand data as an essential input to gauge ICT impact. According to the report ICT is assisting in creating knowledge on many sectors like Agriculture, health, educations, socioeconomic growth etc. In digital communication context it has observed significant increase in use of both fixed and mobile broadband services in both developing and developed world in international scenario. It underlines growth in developed nation has been at a higher rate than developed nations though its usage remains non-measurable. The introduction of high-speed mobile Internet access in an increasing number of countries could further boost the number of Internet users, especially in the developing world. It finds the number of mobile broadband subscriptions surpassed the number of fixed broadband subscribers in 2008 indicating shift in usage pattern. The number of mobile broadband subscriptions refers to subscriptions that have access to a high-speed mobile network. The report finds fixed broadband access is still largely confined to Internet users in developed countries. In the year 2009 broadband penetration stands at 23.3 per cent in developed countries compared to only 3.5 per cent in developing countries. The gap between developed and developing countries appears even wider for mobile broadband penetration, with 38.7 and 3.0 per cent penetration, respectively. The report observes the mobile broadband market in developed countries is dominated by Europe, accounting for 220 million mobile broadband subscriptions (over one third of world's total) [17].
Encouragingly the report observed ICT services have become more affordable worldwide and its usage has increased even in the era of economic downturn. Of the ICT services, fixed broadband service showed the largest price fall. This is followed by mobile cellular and fixed telephone services. The report observed that countries with the highest broadband prices are all ranked relatively low in the ICT development index (IDI) [16, 17] putting forward the view that the services affordability is essential to build an inclusive information society.
It further highlights the fact that Internet plays at home improve educational achievements and accesses role of positive catalyst in socio-economic developments. However, the broadband price gap between developing and developed nations remains enormous and least affordable service in developing world. The gap continues incase of mobile cellular and Internet use though its usages is in increase in developing world. Since these are the platforms used for accessing knowledge generating tools of the day, a look into the related statistics may be revealing [16,17].

8.2 Knowledge Assessment

Knowledge Assessment Methodology (KAM) evolved by World Bank and its indexes are identified to realize inherent benefit in Knowledge Exercise. The KAM was designed by the **Knowledge for Development (K4D)** program to assess a country's preparedness to compete in the knowledge economy using 83 (eighty-three) structural and qualitative variables.
The KAM Knowledge Indexes comprise of **Knowledge Economy Index (KEI) and Knowledge Index (KI)**. The Knowledge Economy Index (KEI) considers whether or not the environment is conducive for knowledge to be used effectively for economic development. (KI) measures a country's ability to generate, adopt and diffuse knowledge. This helps planners of a country to have an opportunity to look into the state of national knowledge exercise, responsible for defining future growth framework and align planning process to reap best benefits out of it [9, 10, 11]. Methodologically, the KI is the simple average of the normalized performance scores of a country or region on the key variables in three Knowledge Economy pillars – education and human resources, the innovation system and Information and communication technology (ICT). ICT score, as registered by World Bank reflects on its preparedness of a country. Of the two knowledge indices in the present context, KI is taken into consideration, which is an indication of overall potential of knowledge development in a given country.

8.3 ITU References

The **IDI (ICT Development Index)** scores registered by ITU (International Telecommunication Union) is culmination of ICT preparedness of a country in terms of infrastructure, ICT use (intensity) and ICT Capability (Skill). IDI reflects on nation's preparedness towards evolving as Information Society.

8.4 Collective Perspective

To allow better comprehension in the following table Knowledge Index scores of top ten KEI ranked countries recorded by World Bank for the year 2009 are charted along with corresponding ICT score. IDI scores of 2008 and 2010, as indicated by ITU of the related countries are also reflected to depict trend of IDI. Scores of India along with other countries with neighboring scores are tabled to present a window view of the scenario. This is likely to present a wider perspective.

KEI Rank 2009	Country	KEI Year 2009	KI Year 2009	ICT Year 2009	IDI Year 2008	IDI Year 2010
1	**Denmark**	9.52	9.49	9.21	7.46	7.97
2	**Sweden**	9.51	9.57	9.66	7.53	8.23
3	**Finland**	9.37	9.39	8.73	6.92	7.87
4	**Netherlands**	9.35	9.39	9.52	7.30	7.61
5	**Norway**	9.31	9.25	9.1	7.03	7.60
6	**Canada**	9.17	9.08	8.54	6.42	6.69
7	**United Kingdom**	9.10	9.06	9.45	7.03	7.60
8	**Ireland**	9.05	8.98	8.71	6.43	6.78
9	**United States**	9.02	9.02	8.83	6.48	7.09
10	**Switzerland**	9.01	9.09	9.68	7.06	7.67
**	********		***	***	***	***
107	**Honduras**	3.21	3.09	3.13	2.72	2.42
108	**Syrian Arab Republic**	3.09	3.57	4.43	3.05	2.66
109	**India**	3.09	2.95	2.49	1.72	2.01
110	**Guatemala**	2.89	2.69	3.31	2.65	2.39
111	**Nicaragua**	2.81	2.60	2.61	2.31	2.09

Table1
***KI, ICT, IDI Scores on 0-10 scale;**
****KI, KEI, ICT Data Source - World Bank; IDI Data Source-ITU**

It has been discussed earlier that World Bank evolved Knowledge Assessment Methodology (KAM) by the Knowledge for Development (K4D) program and indexes therein are identified to realize inherent benefit in Knowledge Exercise. It was designed to assess a country's preparedness to compete in the knowledge economy, using 83 (eighty-three) structural and qualitative variables. It is important to note that according to the study the Knowledge Index (KI) measures a country's ability to generate, adopt and diffuse knowledge; and benchmarks one country's position compared to others in the global knowledge economy whereas the Knowledge Economy Index (KEI) considers whether or not the environment is conducive for knowledge to be used effectively for economic development in the concerned country.

According to the studies in **K4D** program the Knowledge Index (KI) is the average of the rankings of the performance of a country or region in three areas of the so-called Knowledge Economy, namely, education, innovation and information and communications technology (ICT). Thus KI of a country reflects on state of education, new knowledge creation in terms of research and development R&D, patent registration etc and state of ICT exercise therein. ICT in terms of preparedness, use intensity and capability also figures in ITU studies and shapes IDI scores. This makes study of ICT and IDI scores quite interesting.

In the table-1, countries are ranked according to KEI of the year 2009. In that context position of 'Denmark' comes forth at the top vis-à-vis other countries in the world as far as effectiveness of its environment for knowledge usages is concerned though it's KI score is less than Sweden. This indicates that Sweden was more capable than Denmark to generate, adopt and diffuse knowledge though its environment was not as conducive in its usage in the year 2009.

It appears IDI scores are on increase for advanced knowledge generating countries, which indicates infrastructure, skill and intensity is on increase in these countries. Juxtaposing ICT and IDI score gives a window view of two different class of assessment on ICT preparedness of a country. Placing KI next to it helps to reflect on effect of these scores on Knowledge Index. As found in the study, India needs to cover more ground to figure in elite segment. According to the study India figures at 109th position followed by Guatemala, Nicaragua etc. In the same year the ranking continued up to the rank 146, which is held by Haiti. In the following in Table-2, attempt has been made to present perspective of Indian subcontinent and China for the same year i.e. year 2009.

KEI Rank 2009	Country	KEI Year 2009	KI Year 2009	ICT Year 2009	IDI Year 2008	IDI Year 2010
81	**China**	4.47	4.66	4.33	3.23	3.55
88	**Sri Lanka**	4.17	4.04	2.98	2.51	2.79
109	**India**	3.09	2.95	2.49	1.75	2.01
118	**Pakistan**	2.34	2.48	3.39	1.54	1.83
131	**Nepal**	1.74	1.62	0.8	1.34	1.56
138	**Bangladesh**	1.48	1.55	1.53	1.41	1.52
140	**Myanmar**	1.34	1.69	0.7	1.74	NA

Table2
***KI, ICT, IDI Scores on 0-10 scale;**
****KI, KEI, ICT Data Source - World Bank; IDI Data Source-ITU**

According the World Bank study knowledge exercise in Indian Subcontinent has spaces to cover up in terms of education, innovation and information and communications technology (ICT) along with infrastructure development.

Recently World Bank has made data related to KI & KEI for the year 2012 available and it is presented in Table-3. It is evident that there is sharp competitiveness amongst countries in moving ahead to make distinguishable in knowledge society. In the knowledge society first three positions are being held between Denmark, Sweden and Finland with relatively high ICT score. However it appears that capability to generate, adopt and diffuse knowledge, does not always enhance the capability to use it. In Table-3 it is evident that though Netherlands possess same KI score of Finland, in KEI, it scores much less, which finally affects its KEI rank.

KEI Rank	Country	KEI Year 2012	KI Year 2012	ICT Year 2012
1	Sweden	9.43	9.38	9.49
2	Finland	9.33	9.22	9.22
3	Denmark	9.16	9.00	8.88
4	Netherlands	9.11	9.22	9.45
5	Norway	9.11	8.99	8.53
6	New Zealand	8.97	8.93	8.30
7	Canada	8.92	8.72	8.23
8	Germany	8.90	8.83	9.17
9	Australia	8.88	8.98	8.32
10	Switzerland	8.87	8.65	9.20
****	**********	****	****	****
108	Indonesia	3.11	2.99	2.52
109	Honduras	3.08	3.00	3.24
110	India	3.06	2.89	1.90
111	Kenya	2.88	2.91	2.91
112	Syrian Arab Republic	2.77	3.01	3.55

Table-3
***KI, ICT Scores on 0-10 scale;**
****KI, KEI, ICT Data Source - World Bank;**

In this spirited segment Australia, New Zealand and Germany are new entrants, pushing USA, United Kingdom and Ireland out of top ten slots. Slide of countries like USA and UK out of top ten slots, indicate, the state of competitiveness in efforts to improve on state of education, new knowledge creation in terms of research and development (R&D), patent registration etc and state of ICT exercise in it along with efforts in conversion of the same in economic term with the improvement of overall environment. Micro and Macro planners at national level are required to note Indian slide by one more rank with reference to KI & KEI issues, in order to advance efforts to be part of knowledge society.

9. CONCLUSION

Human civilization has gone through various stages like Agrarian, Industrialization, Advanced Industrialization etc. and finally arrived at Information age where knowledge has been identified as an economic entity [5,6,7] as discussed before. An advanced Knowledge Society expected to provide opportunities for knowledge creation and its application for better economic edge. KI and KEI are the measures identified by World Bank, which help in accessing success of a country in efficient production and effective use of knowledge. These measures help to present a perspective, which need not be taken as absolute term, though it is irrefutable that the process helps in taking necessary steps towards knowledge advancement in society. In the present context looking at the table 1, 2, 3 it gets clear that countries with higher ICT and IDI have higher KI, which also vindicate observation made by ITU studies and leads to the conclusion that ICT preparedness affects Knowledge exercise positively leading to a knowledge society. Collectively these studies indicate that to realize higher ICT and knowledge generating capability academic environment, cost of connectivity and other ICT resources needs due attention along with improvement of infrastructure in a country.

FUTURE SCOPE

Technology changes at a fast pace and so does overall scenario, accordingly measures are also adjusted. Thus assessment of Knowledge Society needs to be a continuous process and needs to be realigned with changing scenario.

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A Robust Source Coding Watermark Technique Based on Magnitude DFT Decomposition

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Abstract – ***Image watermarking is considered a powerful tool for Copyright protection, Content authentication, Fingerprinting and for protecting intellectual property. We present in this paper a watermarking algorithm based on block wise changing magnitude of DFT domain. This algorithm can be used as an application for copyright protection. To provide multi-level securities we have first used best self-synchronizing T-codes to encode the watermark. The encoded watermark is then embedded into the cover image using a stego-key. We have analyzed our algorithm against noise such as Salt and Pepper, Gaussian and Speckle.***

Index Terms – Watermark, DFT Composition, Image Processing

1. INTRODUCTION

Watermarking is a branch of information hiding that talks about data embedding in the inconspicuous files or cover objects such as images, video, audio, graphics, texts or packet transmission in a perceptually transparent manner. Digital watermarking is an attempt to solve the growing concerns about proof of ownership, content authentication, copyright violation, tamper proofing, illegal copying and distribution and issues such as fake currency. The basic attributes of watermarking techniques are *Robustness, Security and Undetectability.*

There are three common steps of watermarking techniques viz.,

1. Design of watermark,
2. Watermark embedding and
3. Watermark extraction.

There are various domains of information hiding viz., *spatial domain*, t*ransform domain and spread spectrum domain*. The simplest spatial domain method of watermark embedding is changing the least significant bits (LSB's) of the cover image, but it is not robust to addition of noise or lossy compression. Since the degradation in smoother regions of an image is more noticeable to the human visual system (HVS), it is preferable to hide watermark in noisy regions and edges of images. The transform domain based hiding techniques has not only the potential to achieve higher capacity than the spatial domain based techniques, they are also found to be more robust. Therefore, methods based on transform domain have got more attention than the spatial domain. One can embed watermark by changing the LSB's in the block based transform domain or in the global transform domain. A watermark embedding operation can be carried out in a transform domain, such as *Discrete Fourier Transform* (DFT), *Discrete Cosine Transform* (DCT), *Discrete Wavelet Transform* (DWT), *Singular Value Decomposition* (SVD) *Transform, Karhunen-Loeve Transform (*KLT*)* and *discrete Hadamard Transform* (DHT).

This paper is about information hiding in still images. Most of the research on watermarking is focused on images. Apart from text, images have been used widely as cover objects for the purpose of information hiding as their digital representation provide high degree of redundancy. These techniques are independent of an image formats and hide data in more significant areas of the transformed image. The details of such different watermarking techniques can be found in [3, 4, 12, 15, 17, 19, 20, and 21].

M. Barni et al [7] and R. Dugad [8] have shown DCT or DWT domain semi-blind watermarking schemes to be robust against a number of attacks. However, their method resulting in a weaker detection when a geometric attack (e.g., rotation, translation, and scaling) is tried due to the change in the location of the transform coefficients. Therefore, some researchers [2], [9], [11] have emphasized on DFT-based watermarking because of the properties of the DFT. The DFT of an image is generally complex valued and this leads to a magnitude and phase representation for the image. Most of the information about any typical image is contained in the phase and the DFT magnitude coefficients convey very little information about the image. Thus one would expect that good image compression techniques would give much higher importance to preserving the DFT phase than the DFT magnitude.

Ridzon R and Levicky D [16] have discussed the robust watermarking techniques and proposed one robust digital image watermarking technique based on the discrete Fourier transform and log-polar mapping.

V. Solachidis and I.Pitas [18] have presented an algorithm for rotation and scale invariant water -marking of digital images. An invisiblemark is embedded in magnitude of the DFT domain. The algorithm is shown to be robust to compression, filtering, cropping, translation and rotation.

M. Ramkumar et al [13] have observed that all major compression schemes such as JPEG, SPIHT and MPEG preserve the DFT magnitude coefficients as well as preserve the DFT phase. The other advantage for using the DFT

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magnitude domain for watermarking is lying in its property of translation- or shift-invariance. A cyclic translation of an image in the spatial domain does not affect the DFT magnitude, and because of that, watermark embedding in the DFT magnitude domain remains translation-invariant.

Farid Ahmad [1] has proposed a dual Fourier-Wavelet domain watermarking technique for authentication and identity verification. He has embedded a robust signature and hidden it in a mid-band wavelet subband using Fourier domain bit-embedding algorithm. His method shows the compression tolerance.

In this paper, we present a watermarking algorithm based on DFT magnitude domain using a self-synchronized variable length codes, viz., T-codes for embedding the watermark. In section 2 we explain the proposed algorithm. The experimental results of the algorithm are present in section 3. In section 4, we conclude and give the suggestion on the future scope of this paper.

2. THE PROPOSED WATERMARKING TECHNIQUE

We propose a watermarking technique of block wise changing magnitude of DFT coefficients. The cover image is divided into 8x8 or 16x16 blocks and one bit of secret message (watermark) is embedded into each randomly selected DFT blocks. The maximum payload (capacity) of watermark is equal to the number of blocks constructed in the cover image. Moreover, the watermark (i.e., the hiding message) is imperceptible. The purpose of using Best T-codes in the embedding process has two-fold advantages. First is that we can have better embedding capacity and second is the inherent self-synchronizing property of T-codes. Ulrich [6] has shown that T-codes show the best synchronization performance amongst the most efficient variable length codes and require anything between 1.5 to 3 characters to attain synchronization following a lock loss. Further, A.C.M. Fong et al [5] have shown that T-codes provide better performance for robustness against most common signal distortions. S.K.Muttoo and Sushil Kumar [10] have shown that T-codes give better results of imperceptibility (in PSNR) when they replace Huffman codes in the steganographic methods (jpeg-jsteg/Outguess). The steps of the embedding method are described in the figure 2.1.

The Embedding algorithm is summarized as follows:

…….

0. *Input the Cover image and watermark (i.e., text)*
1. *Divide the cover image into 16x16 (or 8x8) blocks and apply DFT to each block*
2. *Enter watermark (i.e., text or message)*
3. *Obtain the secret message, m, by encrypting the original message using best T-codes*
4. *Let n = size (secret message) and nb= total number of blocks.*
5. *Use PRNG to obtain a permutation of 'nb'- random numbers, say r_i*
6. *While (n <= nb) do*
   For i= 1 to n do
   6.1 Select the random DFT block r_i
   6.2 Embed m_i secret message bit into r_i as follows:
   If m_i = '1'
   Change the block r_i's magnitude by some amount such that
   It should be perceptible
   Else
   'r_i remains unchanged'
7. *Output: Watermarked image.*

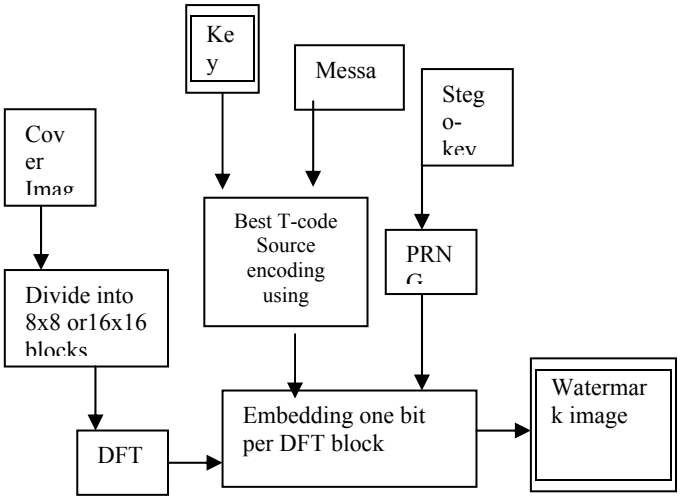

Figure 2.1: "The block diagram for watermark embedding process"

For extracting watermark, we compare each DFT block's magnitude of watermark image with DFT block's magnitude of original image. If they come out to be same, then bit embedded is '0' otherwise it is '1'. The original message is then obtained by decrypting the extracting message using best T-codes. The extraction process is shown in the figure 2.2.

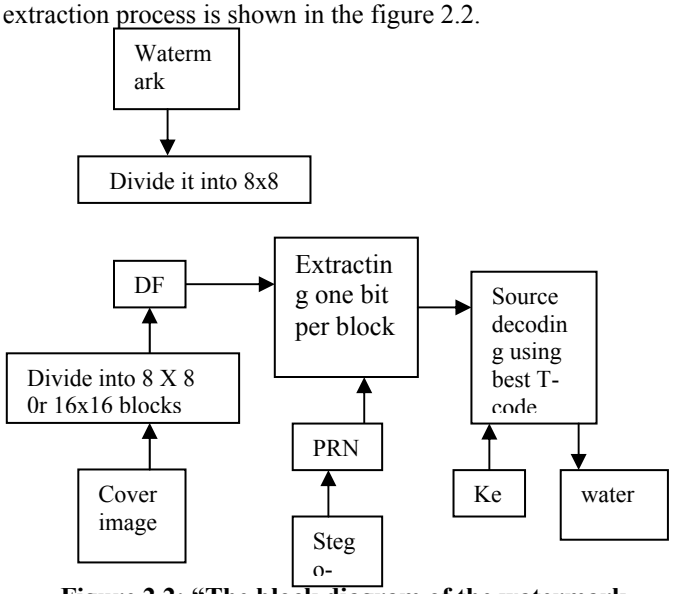

Figure 2.2: "The block diagram of the watermark extraction process"

3. EXPERIMENTAL RESULTS

We have implemented our algorithm on Matlab 7.0 on the 'png' and 'tif' images. The issues of imperceptibly, robustness and security are analyzed.

3.1 Imperceptibility

For imperceptibility, we used the PSNR as a measure of perceptibility. The summary of some of the results obtained are shown in the table 3.1

Length of Secret Message, n	MSE	PSNR Secret message, n
28	0.1657	55.937305
74	0.4971	51.165959
1047	0.8614	48.779914
470	3.1162	43.194567
937	6.1120	40.388943
1023	7.4837	39.389613

[1] $PSNR = 10 \log_{10} (255^2 / MSE)$

$MSE=(1/N)^2 \sum\sum (x_{ij} - x'_{ij})^2$

where x denotes the original pixel value

Table 3.1: "Image: 'lena.png';
Size of image: 512 x 512 x 3"

3.2 Robustness

We have analyzed our technique against Salt & Pepper, Gaussian and Speckle noise. Some of the results are summarized in table 3.2.

Noise	**Noise density/ Variance**	**PSNR**	**imperceptibility**
Salt and Pepper	0.001	33.680459	YES
	0.005	27.354359	Acceptable
	0.01	24.508046	NO
Gussain	0.0001	36.679711	YES
	0.0005	32.201980	YES
	0.01	29.686735	NO
Speckle	0.001	31.795482	YES
	0.01	22.971299	NO

Table 3.2: "Image: 'lena.png' ; n= 1023 ;
PSNR(without noise)=39.423371"

4. CONCLUSION AND FUTURE SCOPE

The algorithm proposed in this paper makes use of DFT magnitude domain for watermark embedding. Watermark can be embedded of capacity equal to the number of blocks created of cover image. Thus, one can have better embedding capacity. From the experimental results as shown above, we observe that the method is robust against adding noise such as Salt and Pepper, Gaussian and Speckle to the extent the image remains imperceptible.

Our extraction algorithms need the original cover image to reveal the hidden text from stego_image, i.e., our scheme is '*cover escrow scheme'*. The other scheme known as '*blind scheme' that* does not require the original cover image to detect the hidden message. It is observed that traditional block transform coding of images may generate artifacts near block boundaries that degrade low bit rate coded images. The Wavelet transforms in the frequency domain techniques have been used because they make the process of imperceptible embedding more effective. Wavelet transform produces much less blocking artifacts than the DCT and they also perform well in image de-noising. Wavelets are found to be well adapted to point singularities but they have a problem with orientation selectivity. They are not efficient in representing the contours not horizontally or vertically. To eliminate the blocking effect new transforms such as *ConTourletstransform* (CTT) and *Lapped transforms* (LOT) have been investigated in the past. These transforms have not yet been explored fully in information hiding. A combination CTT-DWT is suggested to be a good candidate for new compression codec in the literature.

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Figure 3.1: "The original and watermarked image of 'lena.png' for n=1023"

The images with the added noise as given in the table are shown in figure 3.2.

spll8.png

8ns5.png

Figure 3.2: "The above images (noise density) are as follows"
Salt and Pepper: spf.png (0.001), spp8.png (0.005), spll.png (0.01);
Gaussian : gf8.png (0.0001), gg8.png (0.0005), gll8.png(0.001)
Speckle : 8su1.png (0.001), 8ns5.png (0.01))

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A Robust and Efficient Homography Based Approach for Ground Plane Detection

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Abstract – This paper presents a homography based ground plane detection method. The method is developed as a part of stereo vision based obstacle detection technique for the visually impaired people. The method assumes the presence of a texture dominant ground plane in the lower portion of the scene, which is not severe restriction in a real world. SIFT algorithm is used to extract features in the stereo images. The extracted SIFT features are robustly matched by model fitting using RANSAC. A sample of putative matches lying in the lower portion of the image is selected. A fitness function is developed to select matches from this sample, which are used to estimate ground plane homography hypothesis. The ground plane homography hypothesis is used to classify the SIFT features as either belonging to ground plane or not. Image segmentation using mean shift and normalized cut is further used to filter the outliers and augment the ground plane. Experimental tests have been conducted to test the performance of the proposed approach. The tests indicate that the proposed approach has good classification rate and have operating distance range from 3 feet to 12 feet.

Index Terms - Ground Plane; SIFT; Electronic Travel Aid, Homography

1. INTRODUCTION

To get the perception of the environment around them, humans depends upon five senses- vision, hearing, smell, touch and taste. Among these, vision is undoubtedly the most dependable one. Most people cannot imagine what life would be, if they lose it. This is however, a hardcore reality for 45 million people worldwide, who are blind. World Health Organization (WHO) in the year 2010 has estimated that the worldwide count of Visually Impaired (VI) people is about 314 million and 45 million amongst them are completely blind [1].

VI people experience serious difficulties in leading an independent life, due to reduced perception of the environment [2]. The most obvious problem faced by VI people is in navigating the unknown environments without bumping into unexpected obstacles. Thus, obstacle detection is one of the major problems that need to be solved to ensure safe navigation for VI people.

The problem of obstacle detection may often be reduced to the problem of ground plane detection. With the ground plane detected, the other objects can be viewed as obstacles, if they protrude outside of the ground plane. In this paper, we have proposed a homography based ground plane detection method. The developed method is a part of stereo vision based obstacle detection technique developed for VI people. The proposed method assumes the presence of a texture dominant ground plane in the lower portion of the scene, which is not severe restriction in real world. The SIFT matches lying in the lower portion of the image and selected by a fitness function are used to generate a ground plane homography hypothesis. The generated homography hypothesis is used to classify matched SIFT features as either belonging to ground plane or not.

The paper is organized as follows: Section 2 presents an overview of related work. Section 3 explicates the theoretical background of homography. Section 4 presents the proposed approach in detail. The experimental results are given in Section 5. Section 6 makes the concluding remarks.

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2. RELATED WORK

In context of navigation for a visually impaired user, obstacle can be defined as "anything that stops the progression of the user and/or requires the modification of his/her posture." For the past many years, the VI people have been relying greatly on the use of white cane during navigation. However, white cane has an inherent disadvantage. It cannot be used to obtain the information about the obstacles beyond its reach and hence cannot help the user in broad route planning.

Since 1960's, extensive research has been carried out for developing electronic devices, known as Electronic Travel Aids (ETAs), to assist VI people in autonomous navigation [3]. A number of ETAs that make use of radar, lidar and sonar technology [4-11] have been developed. However, their major disadvantages include: interference with the environment, difficult interpretation of the output signals, high power consumption, high acquisition price, poor angular resolution and incapability to detect small obstacles.

Vision-based ETAs have seen tremendous development in the recent years, largely due to the availability of low-cost cameras and compact yet high performance processors that support image processing. Being passive in nature, vision based aids have low power consumption and do not interfere with the environment. These systems work in the direction of capturing the image of an environment and mapping the image into sound or vibratory pulses without undertaking any image processing efforts to provide the information of objects in the scene. In general, background fills more area in an image frame than the objects and hence, conversion from unprocessed images will lead to information overload, with background details masking primary mobility information.

Automatic pre-processing to provide mobility data at a high level of abstraction, by eliminating detailed clutter but retaining essential mobility information, can alleviate the problem of information overload. Ground plane perception is the vital information for human mobility [12]. Gibson in [13] suggested

that "the spatial character of the visual world is given not by the objects in it, but by the ground and the horizon." Molton [14] developed a stereo-based mobility aid for partially sighted people by estimating ground plane using disparity information. Many approaches [15-25] for ground plane estimation for mobile robot and autonomous guided vehicle (AGV) navigation have been investigated by various researchers. These approaches rely mostly on the processing of different features attached to the ground planes: color [18, 19, 20], texture (lane markings) [18], disparity [14, 19, 20], v-disparity [21, 22], motion (optical flow [19, 23]), homography estimation [24, 25]

3. THEORETICAL BACKGROUND

There exist projective relationships between two viewpoints of a scene taken from a stereo rig. The corresponding points in stereo images, taken from uncalibrated cameras, are related by a fundamental matrix. If x and x' are the homogenous image coordinates of the corresponding points $\{x \leftrightarrow x'\}$ in a stereo image pair, **Fx** describes an epipolar line on which the corresponding point **x'** on the other image must lie. For each pair of corresponding points, the epipolar constraint is expressed as:

$$x'^{T}Fx = 0, \quad (1)$$

where F is a fundamental matrix. It is a3 by 3 matrix of rank 2 with seven degrees of freedom, hence it can be recovered from 7 point correspondences.

If a set of points lie in a plane, and they are imaged from two viewpoints, then the homogenous coordinates of the corresponding points $\{x_i \leftrightarrow xi'\}$ in the two images are related by a plane-to-plane projectivity or homography such that:

$$\lambda x_i = H x_i', \quad (2)$$

where **H** is a 3 by 3 matrix representing homography and λ is a scalar. Since equation 2 is valid up to a scale factor, **H** has only eight degrees of freedom and it is normal practice to choose λ such that the element h_{33} in **H** is set to unity. To determine **H**, four corresponding non-degenerated coplanar points are required, since each point correspondence provides two independent constraints, thereby making H determination possible by standard linear methods. However in reality, with the data being non-perfect, more number of point correspondences should be used for the accurate estimation of H.

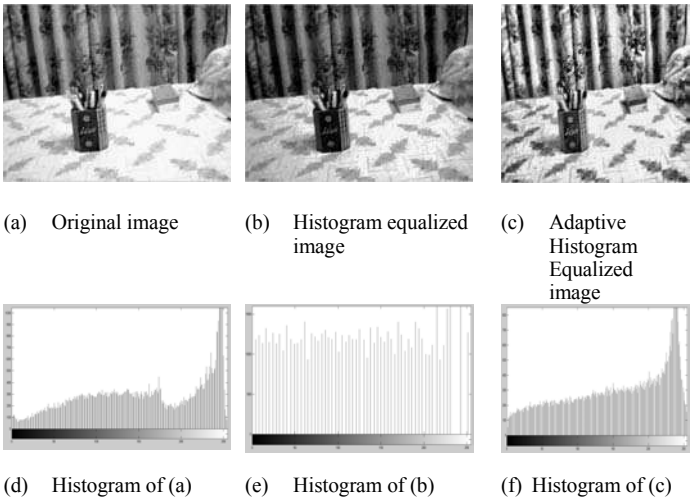
4. PROPOSED APPROACH

The steps involved in the proposed approach are described in the following sub-sections in detail:

4.1 Image Processing

The stereo images grabbed with low cost web cameras, arranged to form a stereo rig, often contain noise. The image noise can be eliminated by using Gauss filter. Contrast- Limited Adaptive Histogram Equalization (CLAHE) algorithm [26] is then applied to enhance the partial contrast and selectively highlight the obvious features, so that the resultant images are more conducive to feature extraction. As opposed to histogram equalization, CLAHE operates on small regions in the image. It enhances the contrast of each region and eliminates the artificially induced boundaries in the neighboring regions by using bilinear interpolation.

Figure 1 shows the result of image preprocessing stage.



(a) Original image (b) Histogram equalized image (c) Adaptive Histogram Equalized image

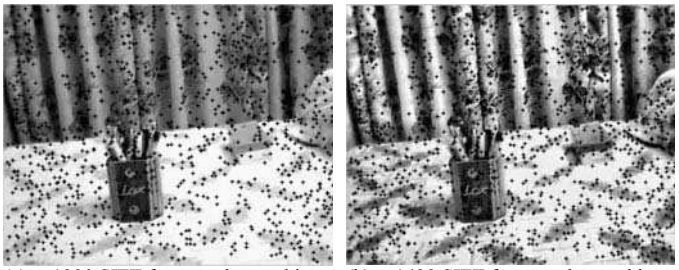
(d) Histogram of (a) (e) Histogram of (b) (f) Histogram of (c)

Figure 1: "The results of preprocessing stage"

4.2 Feature Extraction

The preprocessed image is given to SIFT feature extractor. Lowe proposed SIFT algorithm [27], which consists of four major stages: (1) scale-space extrema detection, (2) keypoint localization, (3) orientation assignment, and (4) keypoint descriptor.

Among various image features like corners, edge features, moment invariants, etc., SIFT features have been an obvious choice for the proposed approach because they are invariant to scale, orientation, and affine distortion, and partially invariant to illumination changes. Using SIFT algorithm, the keypoints extracted for Figure 1 (a) and (c) are shown in Figure 2.



(a) 1290 SIFT features detected in Original image (b) 1439 SIFT features detected in CLAHE applied image

Figure 2: "SIFT features extracted for Figure 1(a) and (c)"

The more number of SIFT features in Figure 2(b) illustrates the advantage of the performed preprocessing step.

4.3 Feature Matching

The SIFT features extracted in the left and right stereo images are matched using the procedure prescribed in [27, 28]. The matches that are too ambiguous are rejected. Matching follows a nearest neighbor approach. The feature F_i in the left image matches feature F_j in the right image, if the distance

$$d(F_i,F_j) < \tau d(F_i,F_k), \text{ for all } k \in I_r;\ j \neq k \quad (3)$$

where τ is a threshold. We have selected the value of the threshold τ to be 0.5. The initially obtained matches are used to

estimate homography and fundamental matrices between pair of images using RANSAC [29]. The set of matches which fits a certain model (homography or fundamental matrix) are considered as inliers for that model. In order to further increase the robustness, outlier rejection rule, called X84 [30], is applied. The robustified inliers are used to re-estimate the parameters of the models. The best-fit model (homography or fundamental matrix) is selected according to the Geometric Robust Information Criterion (GRIC) [31]. The final matches are the inliers from the best-fit model.

4.4 Ground Plane Homography Hypothesis

Since, the algorithm assumes that the textured dominant ground plane lies in the lower part of the scene; a sample of putative matching points lying in the lower part of the image is selected. In our experiment, we have created the sample with the putative matches that lie in the lower 10% of the image. A heuristically designed predefined ground plane mask, as in [20], or a trapezoidal region in the lower central part of the image, as in [32], can also be used to select a sample of putative matches that lies on the ground plane.

The selection of four initial points from this sample to estimate homography is of vital importance. These four initial points will influence the likelihood that they determine a valid homography. The selection of the four initial points from the sample is based on the following criteria [33]:

1. Selected points should not be too distinct.
2. Selected points should not be too close.
3. No three selected points should be collinear or near collinear.
4. Selected corresponding points should have a large disparity in position.

Practically more than four points are required for the accurate estimation of homography matrix H. Algorithm SelectBestN listed in Table 1, is used to select best N-points based on the fitness score, computed for each point according to the mentioned fitness criteria.

1 **Algorithm** SelectBestN(*Ml*, *M'l*, *n*, *Tc*, *Td, N*)
2 r←1
3 Form pairs of points (p_i,p_j),such that p_i, p_j€*Ml*,1 ≤ i ≤ n AND i<j. Select a pair (p_i,p_j) and for every pair repeat step 4 to 8
4 Find midpoint *m* of the point p_i and p_j, fit a line *l* passing through these points and fit a line *q* perpendicular to line *l* and passing through the midpoint *m*
5 Find distances d(p_k,l), d(p_k, q) and d(p_k,m); for all p_k€*Ml* and k≠i,j
6 If distance $d(p_k,m)>Tc$ and $d(p_k,m)<Td$, set $i(k)=1$ else set $i(k) = -1$
7 Compute fitness score for each point $pk: fs(r,p_k)=0.3\times d(p_k,l)+ 0.3\times d(p_k,q)+0.2\times\delta(p_k)+i(k)\times 0.\ m\ 2\times d(p_k)$
8 r←r+1
9 Select r, such that *median(fs(r,:))* is maximum.
10 Sort *fs(r,:)*. Return p_i and p_j for the selected value of r and topmost N-2 points from *fs(r)*

"ALGORITHM to select best N-points based on fitness scores"

Figure 3 shows the result of execution of SelectBestN algorithm. In the figure, the '+' markers are SIFT matches, 'o' markers is the sample lying in the lower 10% of the image. The '⊕' markers are selected by the SelectBestN algorithm for N=6.

Figure 3: "Result of SelectBestN algorithm"

4.4.1 Goodness of Homography Estimate

The determinant of the homography matrix signifies the goodness of a homography estimate [34]. If the determinant tends towards to zero, it suggests the arrival of degeneracy in the selected points. Table 2 lists the values of determinant of homography matrix, average distance error and median of distance errors for three different test executions.

Test Run No. 1				
No. of pts. used for H estimation	**4**	**6**	**8**	**All in the sample**
det(H)	1.04012	0.9950	0.8681	1.2627
Avg(dist(x-Hx'))	0.8857	0.8489	0.8237	1.1525
Median(dist(x-Hx'))	0.9280	0.9406	0.8691	1.1329
Test Run No. 2				
No. of pts. used for H estimation	**4**	**6**	**8**	**All in the sample**
det(H)	1.5900	1.4764	1.0605	1.0569
Avg(dist(x-Hx'))	0.9915	1.3620	0.6228	1.0633
Median(dist(x-Hx'))	0.8415	1.1692	0.5706	1.0265
Test Run No. 3				
No. of pts. used for H estimation	**4**	**6**	**8**	**All in the sample**
det(H)	**0.2389**	1.4246	1.1571	1.0793
Avg(dist(x-Hx'))	**7.5435**	1.4802	0.9292	1.1583
Median(dist(x-Hx'))	**8.4288**	1.3374	0.7643	0.9412

Table 2: "Goodness of Homography estimate for different test runs"

The results indicates that avg(dist(x-Hx')) is very high, if det(H) tends to zero. The homography estimate with minimum average distance error is selected for classifying SIFT features as either "belong to ground" or "not".

4.5 Classification of Sift Features

The corresponding points that lie on a plane shares the same homography, which is different from the homography for

another plane. In reality the homography equation 3 is satisfied only approximately. A pair of corresponding points (x,x') is considered to agree with the ground plane homography hypothesis, H, if for some threshold ε,

$$dist(x,Hx') < \varepsilon \quad (4)$$

Equation 4 is used to classify the matched SIFT features as belonging to ground plane or not. Figure 4 shows the matched SIFT features that have been classified as belonging to ground plane, with the value of ε being kept 5.

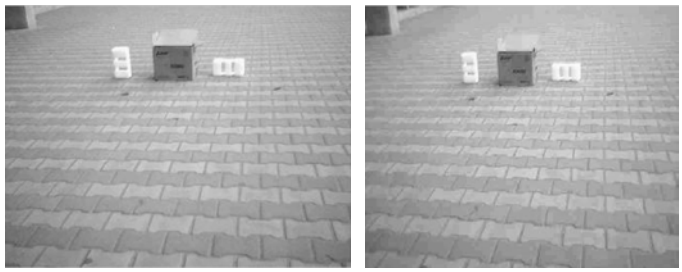
Figure 4: "SIFT features belonging to ground plane"

4.6 Augmenting Ground Plane

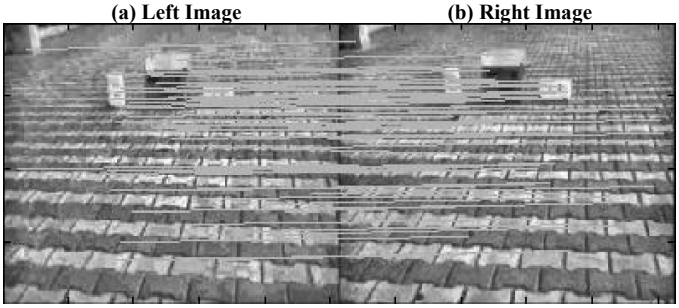
It is likely that that the feature points classified as lying on the ground plane are in the small region of the whole plane. In such circumstances, the region enclosing the classified feature points would not be accepted. We have addressed this problem by using image segmentation algorithm based on mean shift and normalized cuts [35]. The segmented region which encloses maximum number of feature points classified as lying on ground plane is finally labeled as ground plane. This step has an additional advantage of filtering outliers.

5. EXPERIMENTAL TESTS AND RESULTS

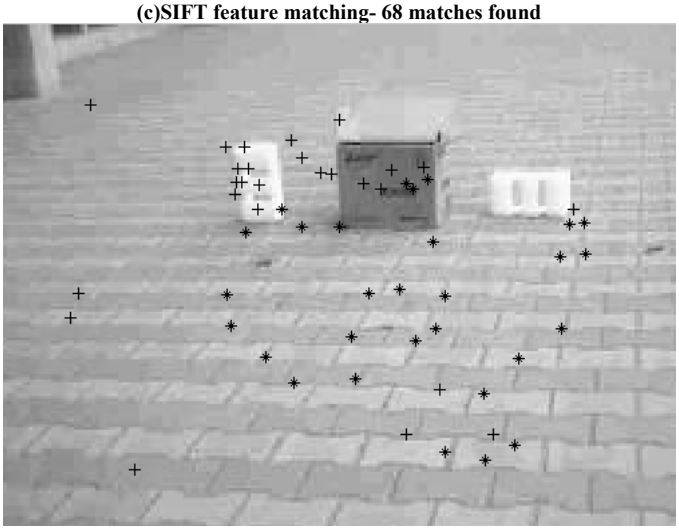
A set of outdoor images were collected from the campus of PEC University of Technology. Figure 5 - 6(a and b) shows some of the samples of stereo image pairs. The images were taken at different times and illumination conditions. Images of different ground planes i.e. tiled, cemented, grassed, etc. and artificial obstacles of different sizes were taken. Enough variation is kept to make the classification task challenging.



(a) Left Image (b) Right Image



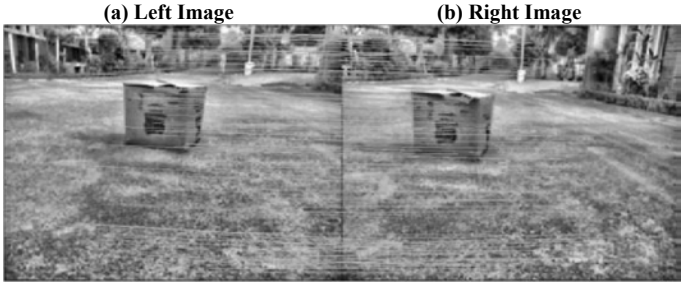
(c)SIFT feature matching- 68 matches found



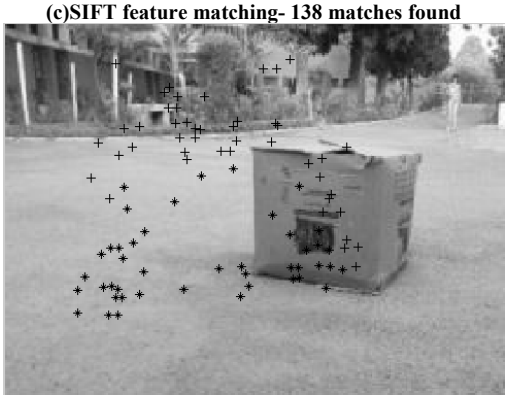
(d) Ground Plane Estimation - Ground Plane features ('*'), Non-ground plane features ('+')

Figure 5: "(a-B) stereo image pair-I, (c) sift matches in stereo images, (d) features classified as belonging to ground plane"

(a) Left Image (b) Right Image



(c)SIFT feature matching- 138 matches found



(d) Ground Plane Estimation - Ground Plane features ('*'), Non-ground plane features ('+' cross)

Figure 6: "(a-B) stereo image pair-II, (c) sift matches in stereo images, (d) features classfified as belonging to ground plane"

On the execution of the proposed approach, the results are collected in form of points marked in the image as points lying on the ground plane and another cluster of non-ground planes. The points which actually lie on ground plane and are marked as ground plane points are termed as true positives. Table 3 contains the result of execution of the proposed approach on the sample image pairs.

Image Pair→	I	II	III	IV	V
Ground Plane points found	30	56	116	28	67
Non-Ground Plane points found	31	52	114	29	68
True Positives	26	55	116	27	52
True Negatives	23	17	41	22	40
False Positives	8	35	73	7	28
False Negatives	4	1	0	1	15
True Positive Rate	86.6%	98.2%	100%	96.4%	77.6%

Table 3: Result of execution on Image Pair III

Figure 7 shows the ROC (Relative Operating Characteristic) curve. Points above the diagonal in the ROC curve clearly indicate that the proposed approach has good classification rate.

Experiments are also performed to determine the distance range, in which, the proposed approach has a good classification rate. At time of grabbing the images, the distance of the obstacles from the camera is noted. The analysis of the proposed approach with respect to distance is shown in form of a graph in Figure 8.

The experimental results indicate that the appropriate operating distance range for the proposed approach is 3 feet to 12 feet. If the obstacle is less than 2 feet away from the camera, the assumption that the lower 10% of the image is dominant which ground plane is violated. If the obstacle is placed very far away from the camera, the features of the obstacle planes are lost and it appears to be the same as the ground plane. Hence, the classification rate of the proposed approach is poor.

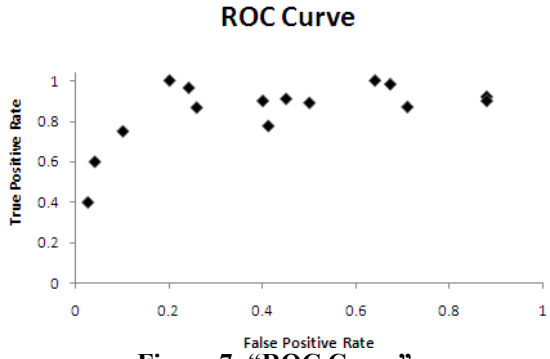


Figure 7: "ROC Curve"

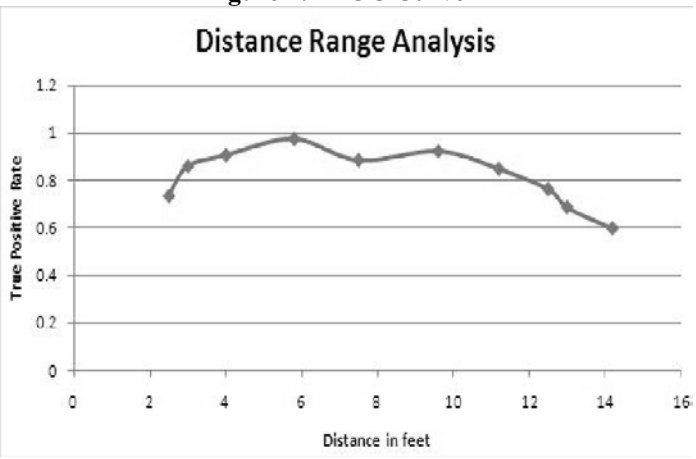


Figure 8: "True Positive rate Vs Distance graph"

6. CONCLUSIONS

The paper presents homography based approach for ground plane detection. The homography is very susceptible to the position of points used for its estimation. The paper presents a point selection algorithm which selects points based on fitness criteria for the accurate estimation of homography hypothesis. A homography estimate with minimum average distance error is used for classifying SIFT features as either belonging to ground plane or not. Generally, the feature points classified as lying on the ground plane are in the small region of the whole plane. This problem has been addressed by using image based segmentation using mean shift and normalized cuts. Experimental tests have been conducted to evaluate the performance of the proposed approach. The performed tests indicated that the proposed approach has good classification rate and operating distance range from 3 feet to 12 feet.

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An Innovative use of Information & Communication Technology (ICT) in Trade Facilitation in India

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Abstract - Directorate General of Foreign Trade, a department of Ministry of Commerce and Industry, Govt. of India, is responsible to formulate, regulate and implement the Foreign Trade Policy through its 36 Port Offices through India.: This is the case study of best e-governance project. This project is highlighted in various e-governance seminars /workshops. This is the first govt. project in which ICT was implemented in 1998. It is soon equipped with Digital Signature and Electronic Fund Transfer facility. The present study is an example of innovative use of Information and communication technology (ICT) for on-line delivery. The present services in the Directorate General of Foreign Trade (DGFT): e-licensing, e-BRC, e-tendering, e-monitoring, e-meeting e-delivery, e-PRC, e-grievance re-addressal etc. The web has been played a dynamic role for reengineering and transformation of trade processes for an efficient, cost effective and seamless trade facilitation.

1. INTRODUCTION

In [1] the survey report highlighted the importance of e-government to improve the public service delivery system to facilitate people in day to day life. E-governance is a tool for developmental activities of any country while in [2] clarify that ICT is a powerful media to transmit the information and knowledge to end user. Most effective and fast solution can be achieved to integrate the technology and planning for economic growth and sustainable human development. [3,4] reflect the idea that ICT may help to government in such a way that new innovative arrangements can flourish instead of traditional institutional arrangements. Such successful initiatives will deliver benefits to citizens and improve the efficiency of government and governmental agencies. [5] represents the role of e-government. [7,9,10,11,13,14,16] represent the web site of Maharashtra, West Bengal, Madhya Pradesh, Haryana, Himachal Pradesh, Rajasthan, and Andhra Pradesh showing the various E-Governance initiatives and applications being implemented in respective states. Mostly websites focus on IT-enabled services and e-governance which include call centre, data processing, back office. [8] Reflects the comparative impact study of many e-governance central government projects out come. processing. [12&15] express the web site features of Ministry of Information Technology including the centralized e-governance projects. The object is included to offer technical services like consultation, awareness among decision makers at the centre as well as state level and guiding them implementing process and policy for effective governance. The IT based services take place for better citizen interface by computerization of Land record, vehicle registration, electricity/water billing, licensing, distance education, health services, online examination, birth/death certificate , e-post, e-court etc through internet. Transparency and free sharing of government database are the major factor to gain the public trust. Henceforth innovative use of technologies is powerful tool to fulfill the requirements of general citizen. In continuation [6] expressed the vital role of online services in around the world. The survey report shows that in many countries e-government initiates and information and communication technologies applications take place for the people to have better public services. Being the catalytic role of innovative technology solutions in government working has gained special recognition. Now a days in the world climate it is very important for the governments to increase electronic service delivery system towards in term of e-government and e-governance. [17] is also a example of ICT evolution in Banking while in [18] ICT strengthen the management and planning of water resources in rural areas. Keeping in view the gist as mentioned in cited reports we have implemented the innovative use of technology in Trade Facilitation in Govt. of India in a systematic manner as:

Directorate General of Foreign Trade (DGFT), an ISO 9001:2008 certified organization regulates and facilitates India's foreign trade by implementing the Foreign Trade Policy and its various Schemes, announced from time to time through Public Notices, Notifications and, Circulars etc. One of the key elements of the policy, apart from providing fiscal and financial incentives to exporters, is to address the issue of high transaction cost in India, so as to improve our global competitiveness. The facilitator role includes resolving trade dispute and attending to exporters / importers grievances.

At the global level, ease of doing business is one of the important parameters on which the status of trade facilitation in a country can be benchmarked. The World Bank's Doing Business Report 2009 and 2010 have pointed out that India is quite behind comparable economies like China, Indonesia and Mexico in this regard. The high transaction time and cost associated with the foreign trade processes have an adverse impact on competitiveness of Indian exports.

With this end in view, the Directorate General of Foreign Trade had established a web based trade facilitation system under which EDI interfaces with the Trading Community and all

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concerned stakeholders in the value chain have been established. This includes Customs, Banks, Trade and Industry and other Government Agencies to facilitate seamless flow of e-documents and information. 'Web' is in-fact the driving engine in this entire endeavor.

2. DIRECTORATE GENERAL OF FOREIGN TRADE (DGFT) INFRASTRUCTURE

Directorate General of Foreign Trade (DGFT) is a multi locational organization, with 36 offices throughout the country. It has Headquarters in Delhi and four Zonal offices at Mumbai, Kolkata, Chennai and Delhi. All locations are interconnected with high speed bandwidth leased line. A backup network facility has also been provided using Broadband.

3. ROLE AS WELL AS FUNCTIONALITIES OF DGFT

The role and functioning of DGFT requires intensive and innovative use of Information and Communication Technology (ICT). The 'Web based solution' has become a core implementation strategy for delivery of an efficient, transparent and easy to access service. The web service includes the following for providing information and implementing transactions;

(i) 'On-line' filing of applications for obtaining all Authorizations through web (B2G model).
(ii) 'On-line' filing of applications for obtaining Importer Exporter Code (IEC).
(iii) Interfaces with various Electronic Data Interchange (EDI) Network Partners.
(iv) Hyperlinked Foreign Trade Policy/Procedure with latest amendments / updates. of status of various applications / authorizations
(v) A Comprehensive Chapter-Wise Directory of Products based on Indian Trade Classification (ITC) for importability / exportability.
(vi) Hyperlinked Foreign Trade Policy/Procedure with latest amendments / updates.
(vii) A Comprehensive Chapter-Wise Directory of Products based on Indian Trade Classification (ITC) for importability / exportability.
(viii) Web based monitoring of status of various applications / authorizations.

4. KEY FUNCTIONALITY THRUST AREAS OF DGFT'S WEBSITE

A snap shot of the DGFT's website is shown in Figure 1.
The functionality thrust of DGFT's website is on the following parameters.

4.1 Citizen Focus

The citizen focus of the web delivery services is achieved through:

1. Accountability and 'SMART' e-Governance Services (Specific, Measurable, Attainable, Realistic, Timely)
2. Transparency in Operations and access to information
3. Continuous improvement in performance and integrity of public services
4. Continuous simplification of Export Promotion and Trade Facilitation measures

4.2 Reach

1. 'On-line' facility for FTP operations available globally, round the clock
2. (24x7x365) through the DGFT's web portal (http://dgft.gov.in) to almost 5 lakh users
3. 36 regional offices of DGFT's spread (but virtually being one) across the country
4. Facilitating of a broad range of 'e-filing' applications under different Schemes like Advance Authorization (AA), Duty Entitlement Passbook (DEPB), Export Promotion Capital Goods (EPCG), incentive/reward schemes i.e. Focus Market / Products, Vishesh Krishi Upaj Yojna, etc.
5. EDI linkages with trade and Industry, Government. Agencies and related EDI community partners i.e., Customs, banks and EPC's etc.

4.3 Scope

(i) Information Access;

1. Foreign Trade Policy / Procedure, Publication of Notifications / Public Notices / Circulars / Trade Notices
2. Indian Trade Classification for Harmonised System (ITCHS) for providing status on importability / exportability
3. Standard Input / Output Norms (SION) for providing details on imports required for export products

(ii) Transaction Facility;

Covers all models of e-governance i.e. B2G, G2G, G2B, G2C and C2G.

B2G: 'On-line' filling of application of authorization/ Importer Exporter Code (IEC) by any business organization
G2G: Message Exchange with Customs, Banks
G2B: Model for 'on-line' filing of applications for authorization / Importer Exporter Code (IEC) and Status thereof
G2C: 'On-line' tracking of application status
C2G: 'On-line' filling of application by individual.

(iii) Monitoring and Tracking

1. Redressal of Trade related queries.
2. MIS available on real time basis.
3. Elimination of fraudulent practices by unscrupulous elements.

5. INNOVATIVE USE OF IT FOR WEB ENABLED APPLICATIONS

'Information Technology' has been innovatively used for web based solutions in DGFT not only to merely Automate and Informate but to Transformate the entire value chain of trade processes.
The Web Enabled Reengineered Work Flow among the various stake holders is shown in Figure 2

The innovative technology intervention has also led to strengthing and almost complete compliance of DGFT's website with the stipulated web guidelines of the Ministry of Information Technology

The innovative use of Information Technology (IT) has been in the following areas:

5.1 "On-line" Filing of Applications:

Flexibility has been provided in 'e-filing' of application through both modes i.e. 'on-line' and 'off-line'. The 'e-filing' facility covers all authorizations on an 'on-line' mode. To maintain high level of server response, an 'off-line' data entry module for Advance Authorizations (AA) and Export Promotion Capital Goods (EPCG) has also been made available on the website. This hybrid approach has enhanced flexibility and eased operations significantly

5.2 The EDI Linkages ('On-Line' Message Exchange with Various Trade Partners);

"Message Exchange" with Customs, Banks and EPC's is Digitally Signed. The Message Exchange design includes a structured and comprehensive monitoring and tracking system comprising of acknowledgment and error message flagging.

1. An appropriate communication technology has been used for different network partners based on users profile, technical and process requirements
2. An 'e-Payment' facility for Authorization fee payment with various banks having Net Banking Facility is available. The number of participating banks is further being expanded to enlarge coverage and scope.

5.3 Technology Up Gradation:

Technology up gradation of Hardware / Software and networking is a continuous exercise. The last up gradation was done in 2011.The present technology profile support / web service is as under:

1. J2EE technology (Applet, Servlet, Enterprise Java Beans, JSP, ASP),XML IBM DB2 as database with digital signature.
   J Builder 2007, J2SDK/J2SEE tools for applications development.
   IBM Web Sphere, Macro Media JRun Web Server for application servers.
2. Rational Suite is implemented for documenting/ designing/ development of the application
3. .The website is being updated using the Extended Markup Language (XML) technology.
4. Whole DGFT Organization is connected with internet / intranet / VPN through very high speed connectivity with NICNET infrastructure.

5.4 Adoption of Comprehensive Technology Management Practices

'On-line' data backup / archiving is done regularly so as to ensure that only 2 years data is available for ready access and the rest is archived. This improves the server response.

1. A Data Warehousing of complete license database from which we may retrieve the data as per the requirement, as and when arises using the Data Mining technology.
2. A Disaster Recovery Site has been installed and is maintained at National Informatics Center (Regional Office, Hyderabad).
3. Site is maintained regularly to ensure 100% uptime.

6. THE IMPACT ASSESSMENT

6.1 Reduction In Transaction Time

1. Cost of preparation of application for an exporter almost brought down to 0.
2. Time required to prepare an application has come down to 5 minutes from 5 hours on an average.
3. Processing time of application has come down to 1 hour instead of 45 days
4. Message Exchange for Authorizations have brought down license verification time from 6 months to automatic instantaneous verification.
5. Status tracking of applications only a click away.
6. Need of paper eliminated completely for application.

6.2 Reduction In Transaction Cost

1. Application can be filed from anywhere
2. Visits of exporters / their representative's to DGFT offices have been reduced to minimum.
3. Trade related documents have been streamlined and reengineered to enhance transparency with no redundancy.
4. Dispensation of physical documents due to integration of digital signature with the system.
5. Application fee has been halved for 'on-line' application.
6. Paper cost brought down by 80%.
7. Physical interface with exporter being reduced further through video conferencing.
8. Journey to a paper less and a green DGFT fast tracked.

7. THE IMPACT SCORE CARD OF TRADE FACILITATION NOW DAYS:

The Impact Score Card			
Activity	Before / After Direct Filing		
	Visits (No.)	Times (Days)	Paper (no.)
Application Filing	2/0	1/@	10/0
Allotment of File No.	1/0	1/@	1/0
Processing of Application	3/0	15-20/1 hrs.	10/2
Issuance of Authorization	3/1	15-30/6 hrs.	10/0
Interchange of Authorization Data with Customs	3/0	7/@	15/0

@; Almost Instantaneous / Automatic

Table1: "Impact Score Card"

8. EXTERNAL RECOGNITION

1. Runner Up for E-Asia Award (AFACT 2005), Taiwan.

2. Participated in ICT solutions for good Governance, 2004 in Hyderabad

9. CONCLUSION AND FUTURE SCOPE

In this paper, we have presented the effects of Innovative Technology in Directorate General of Foreign Trade, Ministry of Commerce and Industries, Govt. of India that support the decision whether an Importer/Exporter get the maximum benefit in minimum time schedule without physical intervention in Governments Offices within transparent environment. The Government of India, department of Electronics and Information Technology, has initiated national e-governance plan for the execution of e-governance projects in the country. In the same manner we have applied the latest techniques in DGFT to move in a successful l e-governance. The fruitful results and outcome has been mentioned to prove the major impact of Innovative technologies in government sector.

***Note:**

Author is posted in Directorate General of Foreign Trade and he is a senior member of Technical Team to automate the DGFT Organization.

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Figure1: "Snapshot of DGFT Website"

Continued on page no. 499

Quantitative Analysis of Spin Hall Effect in Nanostructures

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Abstract - Spin transport in nano structured devices depends on interface resistance, electrode resistance, Spin polarization and Spin diffusion length. Spin Hall Effect (SHE), caused by Spin–orbit scattering in nonmagnetic conductors, gives rise to the conversion between Spin and charge currents in a non local device. Recently, SHE has been observed using non local Spin injection in metal-based nanostructured devices, which paves the way for future Spin electronic applications. In present work we have theoretically analyzed the SHE phenomena based on experimental results obtained till date. We have used the Hamiltonian of two dimensional electron systems with Rashba Spin-orbit coupling. We undertake the quantitative analysis of Spin Hall Effect in low dimensional materials using Spin dynamical equations and Spin Hall conductivity.

Index Terms - Spin transport, Spin Hall Effect, nanostructures
PACS: 75.76. +j, 73.43.-f, 73.63.-b.

1. INTRODUCTION

Spin-dependent transport phenomena in nanostructures are of great interest in the potential applications to Spin electronic devices [1]. Recently much attention has been paid to the Spin Hall Effect, which allows the polarization of electron Spins in nanomaterials [2-6]. In the Spin Hall Effect, electrically induced Spin polarization accumulates near the edges of a channel and is zero in its central region. This effect is caused by deflection of carriers, moving along an applied electric field, by extrinsic [3] and/or intrinsic [4] mechanisms. In a non-magnetic homogeneous system, Spin accumulation is not accompanied by a charge voltage, because two Spin Hall currents due to Spin-up and Spin-down electrons cancel each other [2]. The absence of transverse voltage leads to difficulties in probing the Spin Hall Effect: measuring a charge accumulation is much easier than measuring a Spin accumulation.

Recently, the Spin Hall Effect has been observed both optically [5] and electrically [6]. Valenzuel and Tinkham [6] have reported the electrical measurements of the Spin Hall effect in a diffusive metallic conductor, using a ferromagnetic electrode in combination with a tunnel barrier to inject a Spin-polarized current. An induced voltage has observed that results exclusively from the conversion of the injected Spin current into charge imbalance through the Spin Hall Effect. Such a voltage is proportional to the component of the injected Spins that is perpendicular to the plane defined by the Spin current direction and the voltage probes. In a Spin–orbit-coupled system, a non-zero Spin current is predicted in a direction perpendicular to the applied electric field, giving rise to a Spin Hall Effect [7, 8]. Consistent with this effect, electrically induced Spin polarization was recently detected by optical techniques at the edges of a semiconductor channel [9] and in two-dimensional electron gases in semiconductor hetero structures [10, 11].

Efficient Spin injection, Spin accumulation, Spins transfer and Spin detection are key factors in utilizing the Spin degree of freedom as a new functionality in Spin electronic devices. By analyzing the Spin transport in the structure, we obtain the optimal conditions for Spin accumulation and Spin current. The injection of Spin-polarized electrons and the detection of Spin accumulation depend strongly on the nature of the junction interface.

The theoretical studies on quantum Spin Hall Effect in solid systems are mainly included in metallic graphene and semiconductor system with strain gradient sand. However, since the Spin-orbit interaction in graphene is too small, the theoretical proposals in such systems are difficult to be achieved in experiment. Quantum Spin Hall regime is also very difficult to achieve in semiconductor systems with strain gradients, due to the demanding requirement of a large strain gradient with special configuration and a very low electron density with a clean environment. Spintronics in semiconductors is richer scientifically than Spintronics in metals because doping, gating, and hetero junction formation can be used to engineer key material properties and because of the intimate relationship in semiconductors between optical and transport properties. Spin transport in nano structured devices depends on interface resistance, electrode resistance, Spin polarization and Spin diffusion length. Spin Hall Effect (SHE), caused by Spin–orbit scattering in nonmagnetic conductors, gives rise to the conversion between Spin and charge currents in a non local device.

Optical coherent control method provides a remarkable controllability in the dynamics of atomic Spin states. Furthermore, parameters of cold atomic systems, e.g. atomic number, atom-atom interacting strength, can be well controlled in current experiments. This makes it possible to control the atomic Spin propagation through optical methods, and further demonstrate the quantum Spin hall effect (SHE) in neutral atomic system.

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Also the quantitative analysis of the Spin Hall Effect can be done by measuring electrically in completely non-magnetic systems and without injection of Spin-polarized electrons. A comparative study of requirement tools showing trends in the use of methodology for gathering, analyzing, specifying and validating the software requirements has been used in [17],which has helped us in theoretically analyzing the Spin Hall Effect in low dimensional materials using Spin dynamical equations and Spin Hall conductivity.

2. RESULTS AND DISCUSSIONS

In high mobility two-dimensional electron systems (2DES) that have substantial Rashba Spin-orbit coupling [12], Spin currents always accompany charge currents. The Hamiltonian of a 2DES with Rashba Spin-orbit coupling is given by

$$H = \frac{P^2}{2m} - \frac{\lambda}{\hbar}\vec{\sigma}.(\hat{z}\times\vec{p}) \qquad (1)$$

Where λ is the Rashba coupling constant, $\vec{\sigma}$ refresh the Pauli matrices, m is the electron effective mass, and $\hat{z}$ is the unit vector perpendicular to the 2DES plane. The Rashba coupling strength in a 2DES can be modified by as much as half, by a gate field [13]. The above discussion is valid even when the atomic number, Z, is not equal to one (hydrogen). Recent observations of a Spin-galvanic effect and a Spin-orbit coupling induced metal-insulator transition in these systems [14], illustrate the potential importance of this tunable interaction in semiconductor Spintronics [115].

The dynamics of an electron Spin in the presence of time-dependent Zeeman coupling is described by the Bloch equation:

$$\frac{\hbar d\hat{n}}{dt} = \hat{n}\times\vec{\Delta}(t) + \alpha\frac{\hbar d\hat{n}}{dt}\times\hat{n} \qquad (2)$$

Where $\hat{n}$ is direction of the Spin and α is a damping parameter, that we assume is small. For the application we have in mind, the $\vec{p}$ dependent Zeeman coupling term in the Spin Hamiltonian is $-\vec{s}.\vec{\Delta}/\hbar$, where $\vec{\Delta} = 2\lambda/\hbar(\hat{z}\times\vec{p})$. The Spin orbit interaction is a purely relativistic effect, which is derived from the Dirac equation.

The Spin Hall (SH) conductivity σ_{SH} can be given by the following equation [4]:

$$\sigma_{SH} = -\frac{j_{s,y}}{E_x} = \frac{e}{8\pi} \qquad (3)$$

Which is independent of both, the Rashba coupling strength and of the 2DES density.

But in homogeneous charge and current densities conditions:-

$j_{y,\uparrow(\downarrow)} = \sigma_{\uparrow(\downarrow)}E_y + eD\nabla n_{\uparrow(\downarrow)} \pm \gamma I_{x,\uparrow(\downarrow)}$,

Where Spin conductivity is

$\sigma_{\uparrow(\downarrow)} = en_{\uparrow(\downarrow)}\mu$

where $\sigma_{\uparrow}$($\sigma_{\downarrow}$) is Spin conductivity due to Spin up *(↑)* and Spin down *(↓)* electrons respectively and $n_{\uparrow}$($n_{\downarrow}$) is electrons density of states for Spin up *(↑)* and Spin down *(↓)* alignment.

Current $I_{x\ \uparrow(\downarrow)}$,coupled to the electric field E_0, which is responsible for the Spin hall Effect is

$I_{x,\uparrow(\downarrow)} = en_{\uparrow(\downarrow)}\mu E_0$.

Thus,

$I_{x,\uparrow(\downarrow)} = \sigma_{\uparrow(\downarrow)}E_0$

Show that Spin conductivity is directly depending upon Electric field and the current I.

$\sigma_{\uparrow(\downarrow)} = I_{x,\uparrow(\downarrow)}/E_0$

Which when integrated to get the Hall Voltage ,we gives

$V_H = \alpha_H\omega_N\rho_N j_s$

Where ω_N is the width of the Spin hall device N

Thus Transverse Hall Voltage as a function of the longitudinal Electric field E_0 is plotted as:-

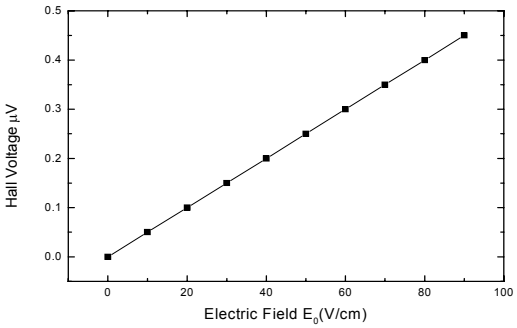

Figure 1: "Traverse Voltage as a function of the longitudinal electric field"

The above result shows an understanding that the average profile curve between the Hall voltage and the longitudinal electric field is normally linear in nature. Certain other Models for the above have also been proposed by the [18], in which novel approaches for developing more efficient relationship model between time and efficiency, have motivated us to model the above work.

In diffusive normal metals, the SHE is known to be induced by the Spin-orbit scattering originating as an extrinsic effect due to impurities or defects [16]. Since the optical detection technique is limited for semiconductor systems, the electrical detection is the only way to access the SHE in diffusive metals. Nonlocal Spin injection in nanostructured devices, provides a new opportunity for observing Spin Hall Effect. If Spin-polarized electrons flow in nonmagnetic electrode, these electrons are deflected by Spin–orbit scattering, to induce Spin and charge Hall currents in the transverse direction and accumulate Spin and charge at the edges.

3. FUTURE SCOPE & CONCLUSION

In nano devices the distribution of the current across the interface depends on the relative magnitude of the interface resistance to the electrode resistance. When the interface resistance is much larger than the electrode resistance as in tunnel junctions, the current distribution is uniform in the

contact area, which validates the assumption of uniform interface current. However, when the interface resistance is comparable to or smaller than the electrode resistance as in metallic contact junctions, the interface current has inhomogeneous distribution with a high current density around a corner of the contact. Using the nonlocal Spin injection, a pure Spin current is created in nonmagnetic conductors, so that we have the opportunity to observe the Spin-current induced SHE in nonmagnetic conductors via the Spin–orbit scattering by nonmagnetic impurities. The observation of the SHE provides direct verification of the existence of Spin current flowing in nonmagnetic conductors. In a reversible way, the electrical current creates the Spin current via the SHE, which provides a Spin-generating source without the need to use ferromagnetic materials. The nonlocal Spin injection also makes it possible to realize a nonlocal Spin manipulation. The advantages of nonlocal lateral structures are flexibility of the layout and the relative ease of fabricating multi terminal devices with different functionalities. The development of nonlocal Spin devices is a new challenge in the research field of Spin electronics.

This result opens up a new possibility to use normal metals with high Spin-orbit coupling as Spin current sources operating at room temperature for the future Spintronic applications.

ACKNOWLEDGMENTS

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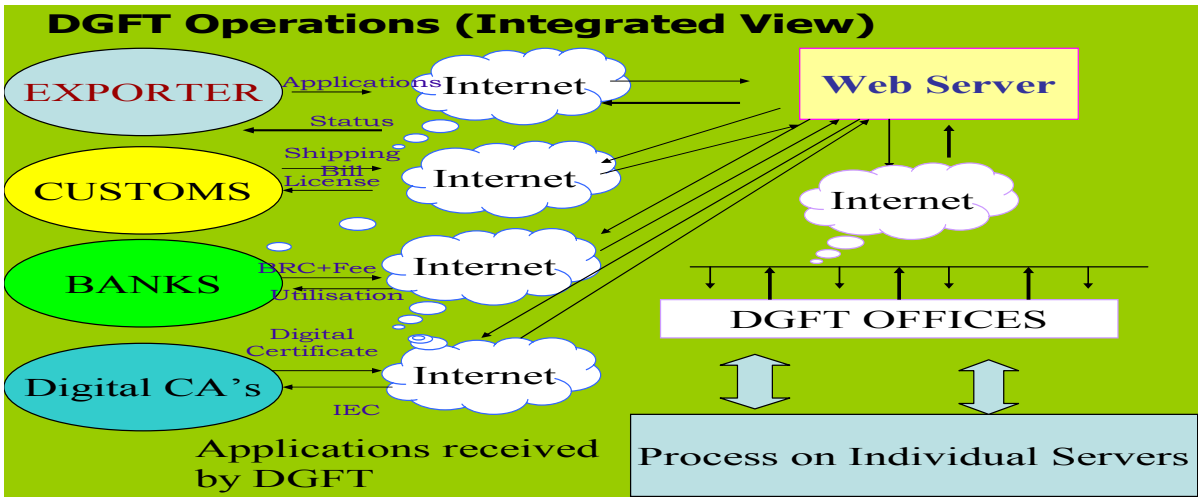

Figure2: "Electronic Data Interchange Flow Chart"

Simulation Study for Performance and Prediction of Parallel Computers

Neeraj Kumar

Submitted in January 2012; Accepted in June 2012

Abstract - ***The issue of performance evaluation and prediction has concerned the users throughout the history of computer evolution. In recent times the parallel computer is gaining popularity as an effective solution to low cost supercomputing. In this study we discuss a simulation study, performed for evaluating the performance of parallel computers connected in different topologies.***

Index Terms - ***Performance measures, Processor utilization, System utilization, Throughput***

1. INTRODUCTION

The future need of much more powerful super computation asks for parallel (digital) computers, containing a large number of fast processors that can cooperate quickly and efficiently. In parallel processing, high performance data processing and data flow are of equal importance. In practice so far, loss of efficiency often happens for the technical reason that the communication system of a parallel computer has not enough capacity. Lack of communication capacity will result in transfer bound processing instead of computation bound processing. Loss of efficiency also often happens because a parallel algorithm is still in the early stage of development. That makes it difficult to define the architecture and programming of a parallel computers such that, efficient implementation of parallel algorithms is possible in a wide range of applications. Moreover, the applicability of parallel computation is hampered, since the programming in parallel computation is still more difficult than programming in serial computers.

The need for computer performance evaluation exists from the initial conception of a system's architectural design to its daily operation after installation. In the early planning phase of a new computer system product, the manufacturer usually makes two types of predictions. The first type is to forecast the nature of applications and the levels of system workloads of these applications. Here, the term workload means the amount of service requirements placed on the system. The second type of prediction is concerned with the choice between architectural design alternatives, based on hardware and software technologies that will be available in the design period of the planned system. Here the criterion of selection is known as cost performance trade off. The accuracy of such prediction rests, to a considerable extent on the capability of mapping the performance characteristics. Such translation procedures are by no means straightforward or well-established. After the architectural decisions have been made and the system design and implementation started, the scope of performance evaluation becomes more specific. The interactions among the operating system components—algorithms for job scheduling, processor scheduling, and storage management must be dealt with, and their effects on the performance must be predicted. Comparing the predicted performance with achieved performance often reveals major defects in the design or errors in the system programming. Now, it is universally accepted that the performance evaluation and prediction process should be an integral part of the development efforts, throughout the design and implementation activities.

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2. MEASURES OF PERFORMANCE

When it is said that the performance of the computer is great, it means, perhaps, that the quality of service delivered by the system exceeds the expectation. But the measure of service quality and the extent of expectations vary depending on the individuals involved, eg, system designers, installation managers, terminal users, etc. If an attempt is made to measure the quality of computer performance in the broadest context, then issues like user response (as well as the system response), ease of use, reliability, user's productivity, etc must be considered as the integral parts of the system's performance. Since the performance analysis cannot avoid issues that are ultimately behavioural, the scope of this is discussed only in terms of clearly measurable quantities. This is done in the conventional way as, for instance, the signal-to-noise ratio probability of decoding errors as measures of performance of communication systems.

The performance measures can be classified into two broad categories:

(i) user oriented measures, and
(ii) system oriented measures.

The user oriented measures include such quantities as the turnaround time in a batch system environment and the response time in a real time and/or interactive environment.

The turnaround time is the length of time that elapses from the submission of the job, until the availability of its processed result. In the similar way, in an interactive environment, the response time of a request, represents the interval that elapses from the arrival of the request until its completion in the system.

Usually jobs are categorized according to their priority classes. Many factors may determine the assignment of priority to a job: the job's urgency, its importance and its resource demand characteristics and utilization.

Throughput is defined as the average number of jobs processed per unit time. It provides the degree of productivity that the system can provide. But in this case, throughput is not an adequate measure of performance; rather it is a measure of system workload.

2.1 System Utilization

In an execution cycle, all the processors may not participate in execution and may be idle throughout an execution cycle, waiting for results from other processors. The utilization of the system in terms of the number of processors used in an execution cycle is quantified by the parameter S_u, which is referred to as system utilization.

An algorithm has been considered which is executed in r cycle on P processors. Suppose, in an execution cycle of t_1 time units, P_1 processors are used, and in the next execution cycle of t_2 time units, p_2 processor are used , and so on then,

$S_u = (P_1*t_1+P_2*t_2+\ldots\ldots+P_r*t_r)/(P*(t_1+t_2+\ldots\ldots+t_r))$.

2.2 Processor Utilization

When the sub-domains assigned to different processors are not equal, then some processors finish computation earlier than others. As synchronization takes place at the end of every cycle, these processors wait for others to finish. This leads to idling and under- utilization of some processors which is quantified by the parameter P_iu for processor i. It characterises the load balancing of the system. Perfect load balancing occurs when the sizes of the sub-domains assigned to all the processors are equal, i.e, when $P_iu=1$, for i=1,2,….,p (where P is the number of processors in the system).

2.3 Inter-Processor Communication Time

In a message passing through multiprocessor, if $t_{start-up}$ represents the message start-up overhead or latency; t_{send} represents transmission time (which is inverse of the link bandwidth); 'k' bytes between two neighbouring processor involve a communication time, $t_{comm}=t_{start-up}+t_{send}*k$.

When the communication is not between two near neighbours, the communication time is estimated by assuming that it takes place in hops, and each hop corresponds to a near neighbour communication. The communication time between two processors is $n*t_{comm}$, where n is the number of hops by which the two processors are separated.

3. ANALYSIS OF PARALLEL ALGORITHMS

Once an algorithm for a new problem has been developed, it is usually evaluated using the following criteria: running time, number of processor used and cost[1].Besides these standard metrics, a number of other technology related measures are sometimes used when it is known that the algorithm is destined to run on a computer based on that particular technology.

Running Time

As the speed is emerging to be the main reason behind the growing interest in the field of parallel computers, the most important measure of a parallel algorithm is, therefore, the running time. According to AK1[1], running time is defined as parallel computer, that is, the time elapsed from the moment the algorithm starts to the moment it terminates. If the various processors do not begin and end their computation simultaneously, then the running time is equal to the time elapsed between the moment the first processor to begin computing starts and the moment the last processor to end computing terminates.

In evaluating a parallel algorithm for a given problem, it is quite natural to do it in terms of the best available sequential algorithm for that problem. Thus a good indication of the quality of a parallel algorithm is the 'speed-up' it produces.

This is defined as

Speed-up= (worst-case running time of fastest known sequential algorithm for the problem)/(worst-case running time for the parallel algorithm).

3.1 Number Of Processors

The second most important criterion in evaluating a parallel algorithm is the number of processor it requires to solve a problem. It costs money to purchase, maintain and run computers. When several processors are present, the problem of maintenance, in particular, is compounded, and the price paid to guarantee a high degree of reliability rises sharply. Therefore, the large the number of processor an algorithm uses to solve a problem, the more expensive it becomes to obtain the solution. For a problem of size n, the number of processors required by an algorithm, a function of n, will be denoted by p(n). Sometimes the number of processor is a constant independent of n.

4. IMPLEMENTATION

In traditional implementation of parallel programs, there is often no way of ensuring that the code implements designer's intentions. For example, a simple typographical mistake during coding can cause two processor to communicate when they should not, leading to disastrous, unpredictable consequences. If the design specifications could somehow be fed directly to the language processor, this unintended communication could be diagnosed syntactically. Inorder to be viable, the design must be formally defined as a computer language.

5. DESIGN OF SIMULATOR

In this simulator, a multiprocessor environment is simulated to evaluate the performance of different standard computation under various topologies. All the standard topologies like bus, ring, torus, hypercube, mesh, and tree are considered.

The simulation is done in c language

5.1 Assumptions

The model proposed here for performance prediction assumes that all inter processor communication times can be estimated a priori and that there are no unpredictable queuing delays in the system. An input file, having two fields containing

processor-ID name and process, and also the communication file is available. It is also assumed that any process can complete its message passing in one communication cycle if the route is free and the receiving process is ready.

5.2 Model

The input to this simulator is given after balancing load with a suitable load balancing technique. Here at each processor two queues are maintained: a ready queue, and a communication queue. In the beginning the ready queue at each processor contains all the processes assigned to that processor and the communication queue is kept empty. The round_ robin job scheduling technique is followed at each processor, ie, each process at a processor, is given a time slice for execution. An execution cycle is followed by a communication cycle. In the processes requiring communication among themselves communicate. Before any of the two processes communicate, first the links connecting them through the shortest path are examined. Then the communication queue of the partner processor is searched for the partner process. If it is found there, the communication delay is added to the respective counters and the partner process is removed from the front of the ready queue and is placed at the rear of the ready queue. When all the queues are exhausted then the program terminates. Computation time is added to each process at the end of each computation cycle. It also calculates time of completion of each queue. That is done by adding execution time of all the processes at each processor separately.

The different parameters and structures are described as follows.

Structure processor includes

(i) Current state of processor, ie, 'o' for every 1 for ready and 2 for idle.
(ii) Time_ stamp, clock, link clock for each link; and
(iii) Three process queues. Each queue has its own count.
  (a) Ready_ queue of active processes waiting for communication.
  (b) Communication_ queue of inactive processes waiting for communication.
  (c) Wait queue of inactive processes waiting to be creates as threads.

Proc_ array is dynamically allocates array of processors.

The declaration for the above is made as follows.

```
Struct processor {
Int current_ state;
Unsigned double time_ stamp , clock,*link_clk;
Int ready_process_count,comm_process_count,
Wait_process,count;
Struct process*ready_q_tl,*wait_q_t,(* comm._q_tl;
        }**proc_arr;
```

Structure process includes

(i) Process_ id identification of the process;
(ii) Priority of the process : 1 if urgent else 0;
(iii) Current state of process 0 if over and 1 if ready;
(iv) Partner_ proc : communication partner processor

Partner_ process: communication partner Process;

(v) Instruction queue and instruction count; and
(vi) Pointer to the 'next' process in the linked list.

The structure process is defined as follows.

```
Struct process {
Int priority, process id, inst_ count state; current state;
Int partner_ proc, partner_ process;
Unsigned double clock;
Struct process*next;
Struct inst_list,*instr_ hd, *instr_ tl;
};
```

The structure instruction list includes

(i) Type: integer value indicating the type of instruction;
(ii) Params array : parameter required for that instruction; and
(iii) Pointer to the next instruction in the linked list.

The declaration for list_ list is given as follows:

```
        Struct instr_ list {
        Int type;
        Int params4;
        Struct instr_ list*next;
        };
```

Other variables declared include t_ calc which store the total computation time, ie, the time required to run the same application on a single processor.

Initialize ( )

The initializing subroutine is a semi- interactive subroutine which initializes all parameters used afterwards by the simulator. Here the number of nodes/ processors type of topology

Processor used and its frequency are taken as input. Also the clock used is initialized. All the process counts are also initialised.

get_link(int sp.int dp)

This subroutine takes the destination and the source processor as input (as well as topology)and returns communication link between those two processors. Here popular topologies like mesh, star, hypercube, tree, torus and wk_recursive are consider as well as the logic topologies like ring, pipeline, etc.

read_input(cha*filename)

This function reads the input file given in command line argument. Here declaration of various dummy statements is given which is the output file of the parser. Parser replaces the actual parallel C statements by these dummy Statements considering the worst case of execution. Here the queues for different processors are maintained to be used by the simulator. There are several smaller procedures doing different tasks.

void create(int*pro_arr)
This creates another (thread) process. This thread which was initially stored in wait queue and is moved to read queue. Delay is added to the process and processor clock, and the process input in the ready queue end.
void send(int*par_arr)
This performs the communication operation 'send'. At first the partner processor of processes is updated. Then the communication queue of the partner processor is reached to find out whether it contains partner process or not. If it is able to find partner process, then corresponding communication delay is added to both the processes. The partner processes is removed from the communication queue of the partner processor or is put in its ready queue, and the ready queue and communication queue of the partner process are updated. On the other hand, if it is unable to find partner process in the communication queue of the partner processor then the current process is put in the communication queue of the current processor. If it is able to find the partner processor, corresponding link delays are added, and the current process is put in the ready queue end.
void receive(int*pro_arr)
This function performs the communication operation 'receive'. Here, first the communication queue of the partner processor is reached for the partner process. If it is found, then communication delay is added to both the processes. The partner process is removed from the communication queue of partner processor or is put in its ready queue. The communication queue and ready queue of partner process are updated. If unable to find the partner process in communication queue of partner processor then the current process is put in the communication queue of the current processor. If it is able to find the partner process, the corresponding link delays are added and the current process is put at the ready queue end (the text is available with the author).
There are several other procedures to add computational delay, communication delay, link delay, etc and procedure link send it changes the state of a process and removes it from the queue.
Simulate ( )
This module does the simulation work and a file is opened to write the instructions as executed by simulator. It starts on processor zero. If the time_stamp of current processor is greater than allotted time slice or if it is ready process queue then the procedure processor_schedule is allowed else procedure process_schedule is called.
The processor_scheduler finds the processor with minimum clock as the new current processor. It follows a linear search for the above purpose. The process_scheduler finds the process on the current processor having urgent priority and places it in ready_queue head of the current processor so as to execute it next (details available with the authors). The simulator continues till all instructions of all the processes are over.
Statistics ( )
This procedure calculates all the statistical information and stores them in a file. Time is estimated for the application to run on a single processor, the overall efficiency. Maximum of all processor clocks (details available with the author) is also calculated.

Algorithm

```
Begin
initialize(     ) // Initializes various parameters and variables.
read_input      // Read input from the designated file.
simulate        // Start the simulation.
statistics      // Transfer the desired results to a
                   predetermined file.
End
```

6. DISCUSSION

In this model, the processor executes a computation step and after finishing, they synchronize and perform data exchange in a cycle. If during execution of an algorithm, all the processors are performing computations in all cycles then the system utilisation is 1. However, it is found that in some algorithm all the processors may not participate in computation in all the cycles, as some processor may be waiting for the results generated by some other processors. The value for such algorithms is less than one.
The level of details required in the validation of a simulator should depend on how that simulator is to be used in decision making. If the performance measure thus obtained has some mean value (eg, CPU utilization, the average response time), then the notion of significance level and confidence interval should be applied to quantify the statistical significance of the difference between measured and simulated effects. The analysis of variance technique can also be used to test the hypothesis.

7. CONCLUSION

The model discussed here determines the performance of a static system. With some modifications, it can be made to work in dynamic environment also. The model discussed has got some limitations. Its advantage is that it helps smaller processes to complete execution by providing them time slices. In many cases the intermediate results provided by such processes is used by the other processes to continue execution. Since in most cases, parallel computers are used for similar kind of jobs repeatedly, by monitoring the communication pattern, the execution cycle can be varied to reduce the context switching overhead.

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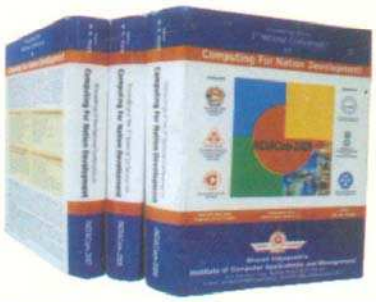

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